

Braindrop: A Mixed-Signal Neuromorphic System that Presents Clean Abstractions

Kwabena Boahen* Bioengineering & Electrical Engineering Stanford University

*Cofounder & Chief Scientific Adviser, Femtosense Inc. 26 March 2019

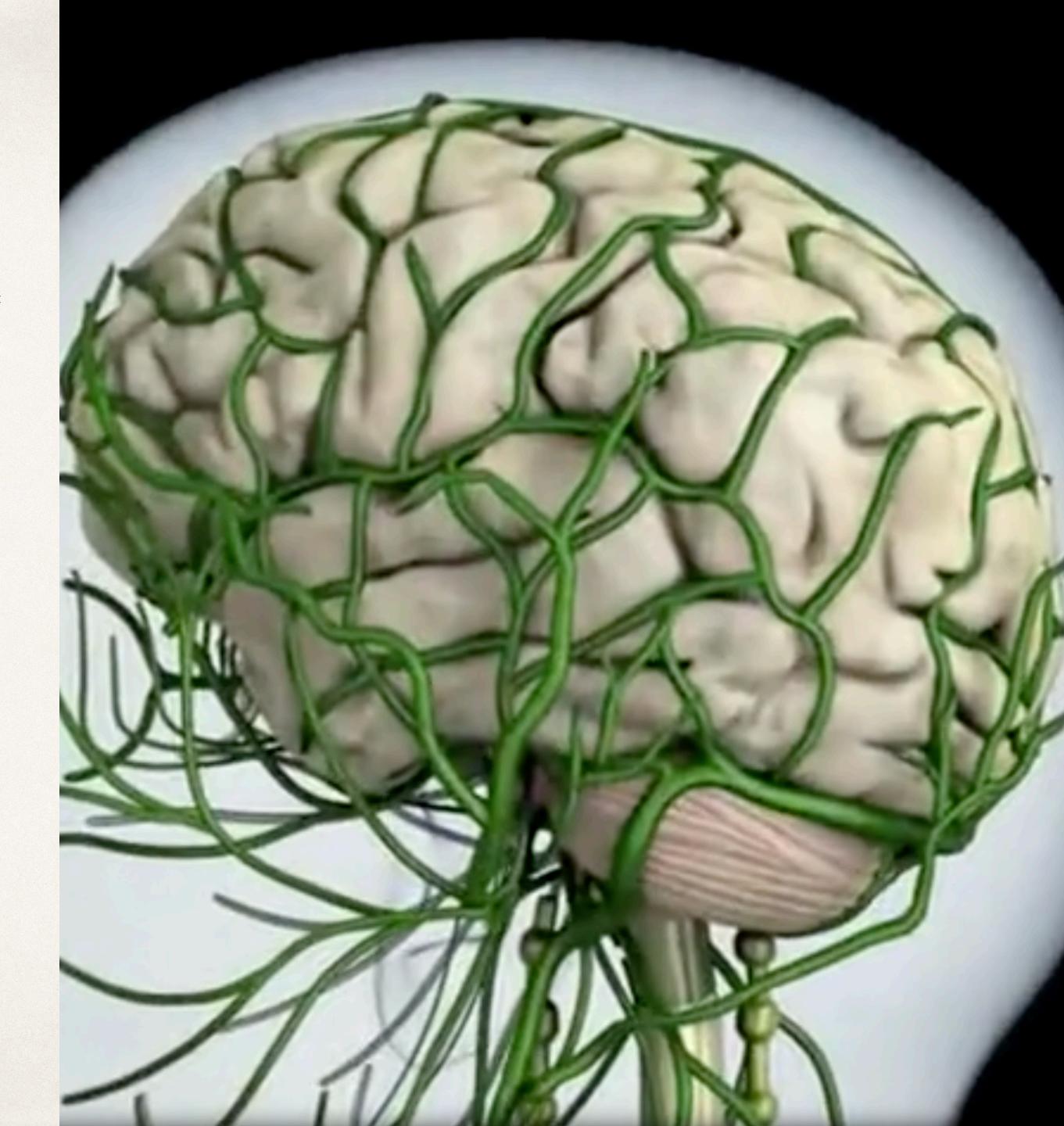
Deep learning is huge —in the cloud

- Backprop learning is powerful
 - Networks <u>deep in space or time</u>
 - Space is discretized into <u>layers</u>
 - Time is discretized into <u>steps</u>
 - Unit's output must be <u>differentiable</u> (with respect to outputs of units feeding it)



Backprop's constraints limit design-space

- Cannot take advantage of:
 - Physical <u>space</u> (its continuous)
 - Real <u>time</u> (its also continuous)
 - Non-differentiable signals
 (e.g., <u>spikes</u>)



How do we relax its constraints? (Part I)

- Map functional abstractions onto physical ones
- Two existing examples:
 - Neural Engineering Framework (Eliasmith & Anderson 2003)
 - Predictive Coding Framework (Deneve et al. 2014)

Neural Engineering

COMPUTATION, REPRESENTATION, AND DYNAMICS

IN NEUROBIOLOGICAL SYSTEMS

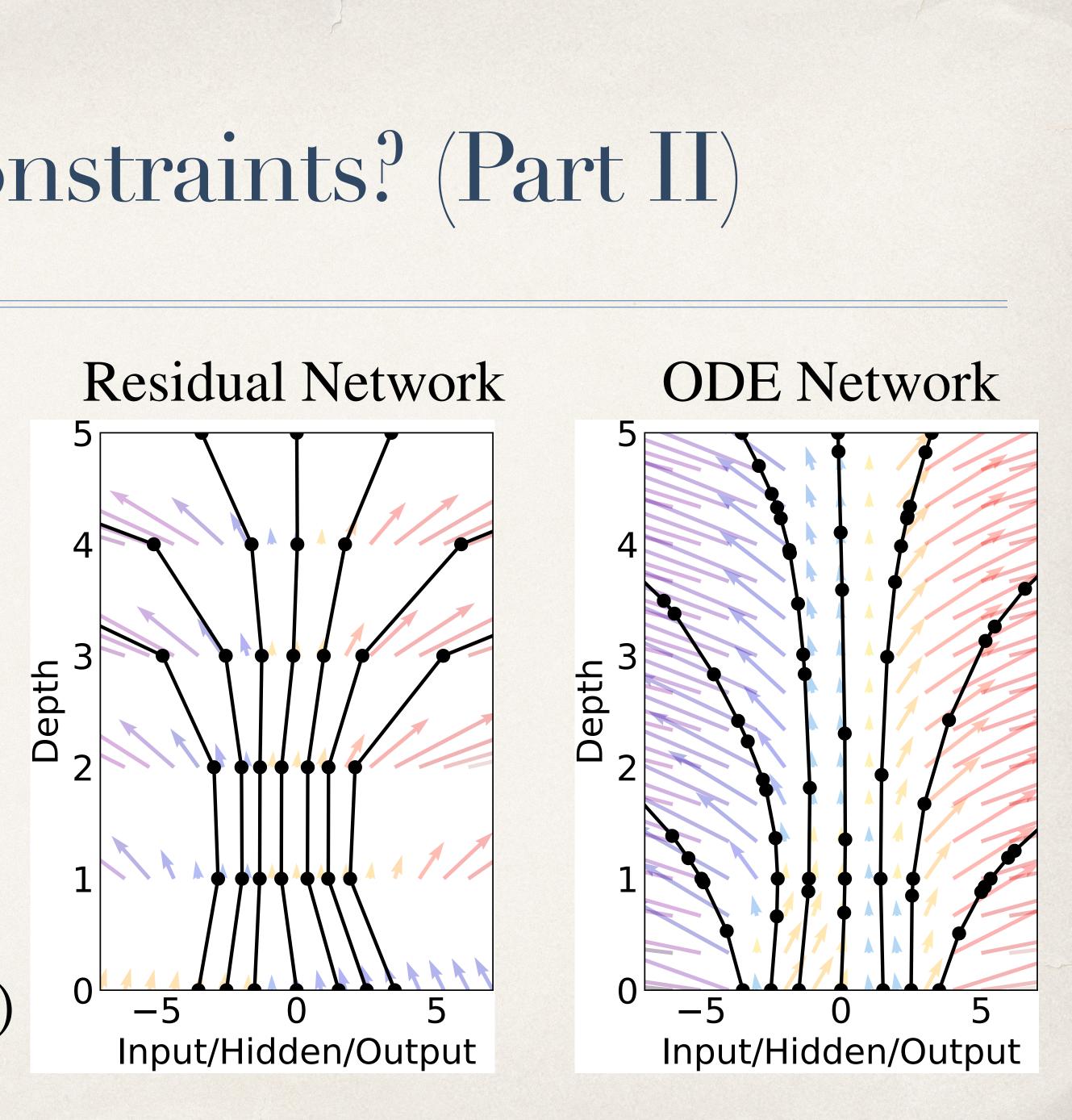


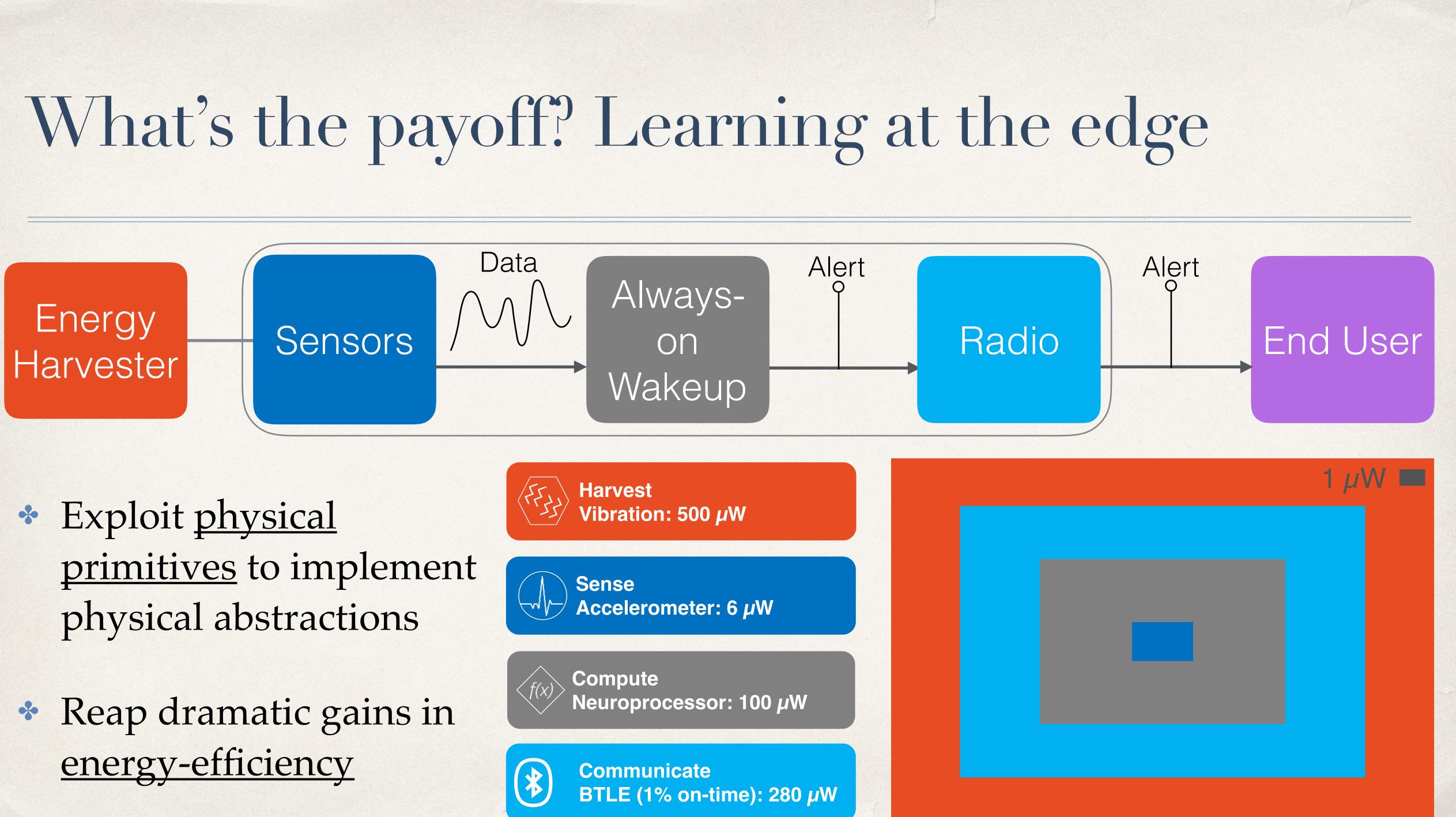


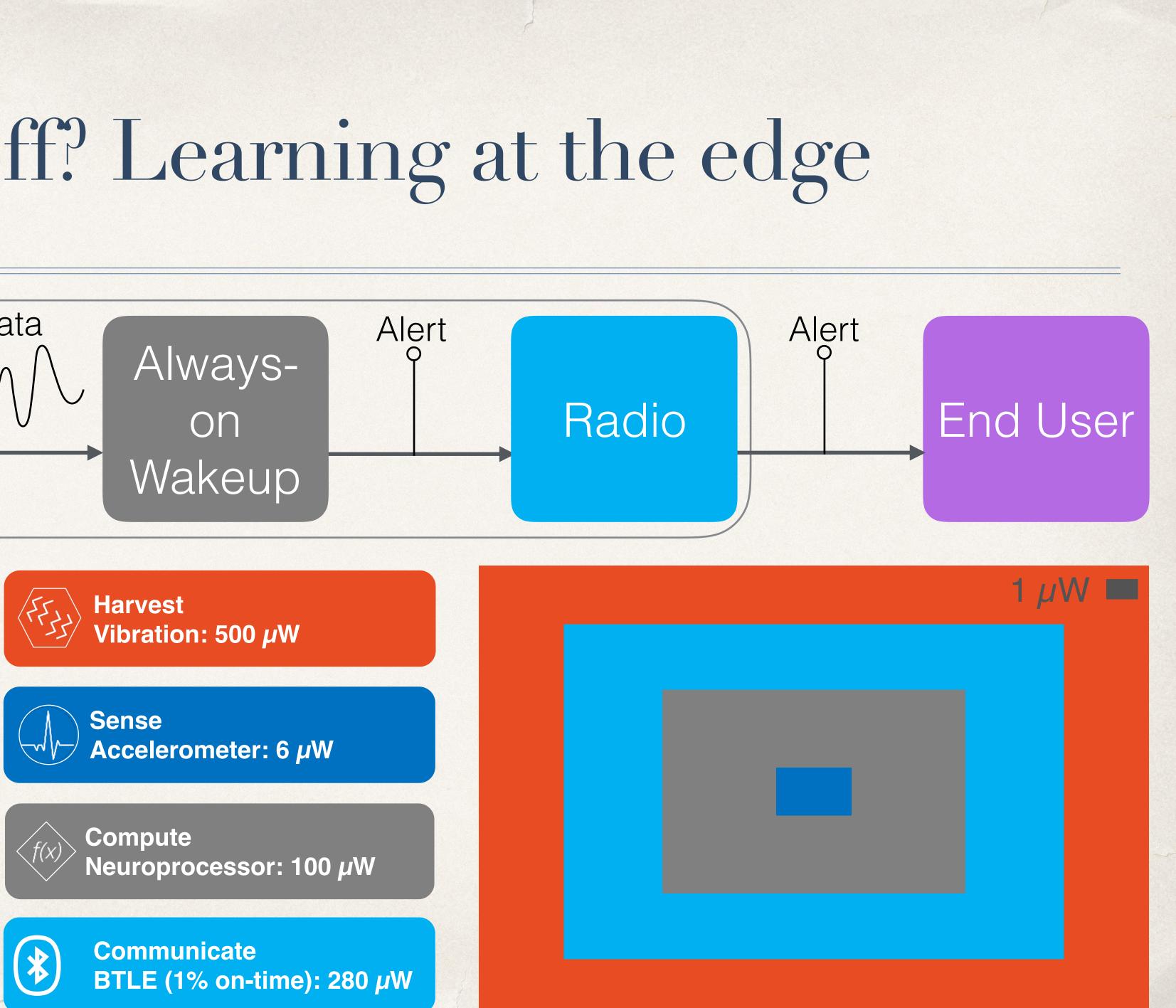


How do we relax its constraints? (Part II)

- Train networks continuous in time and space
 - Known as <u>dynamical systems</u>
- An existing example:
 - <u>Neural Ordinary Differential</u>
 <u>Equations (Duvenaud et al. 2018)</u>





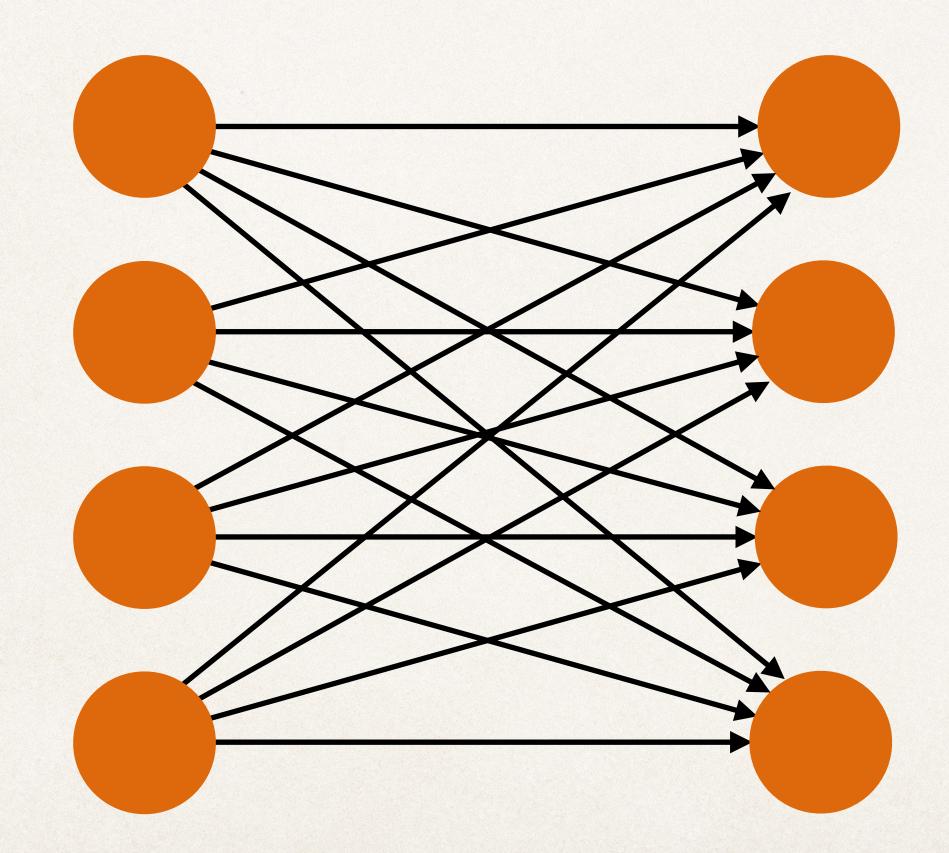








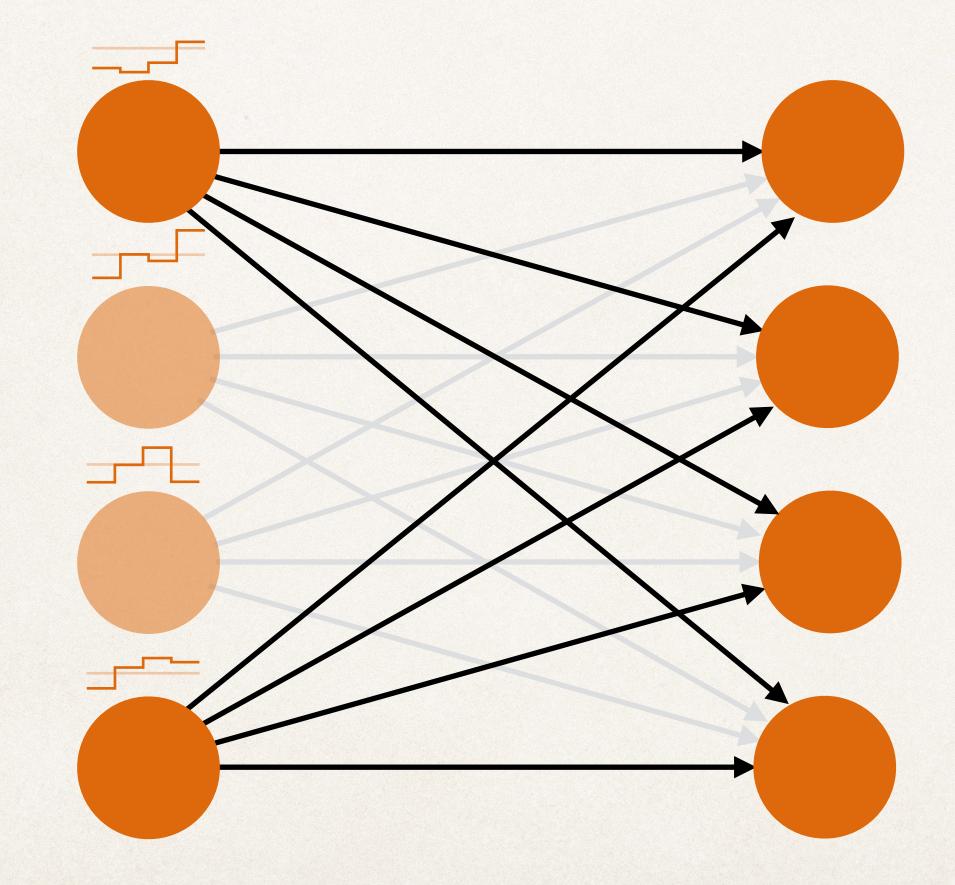
Minimizing energy



$E_{op} = N_{active} N_{conn}$ $= (\rho_{active} N)(\rho_{conn} N)$



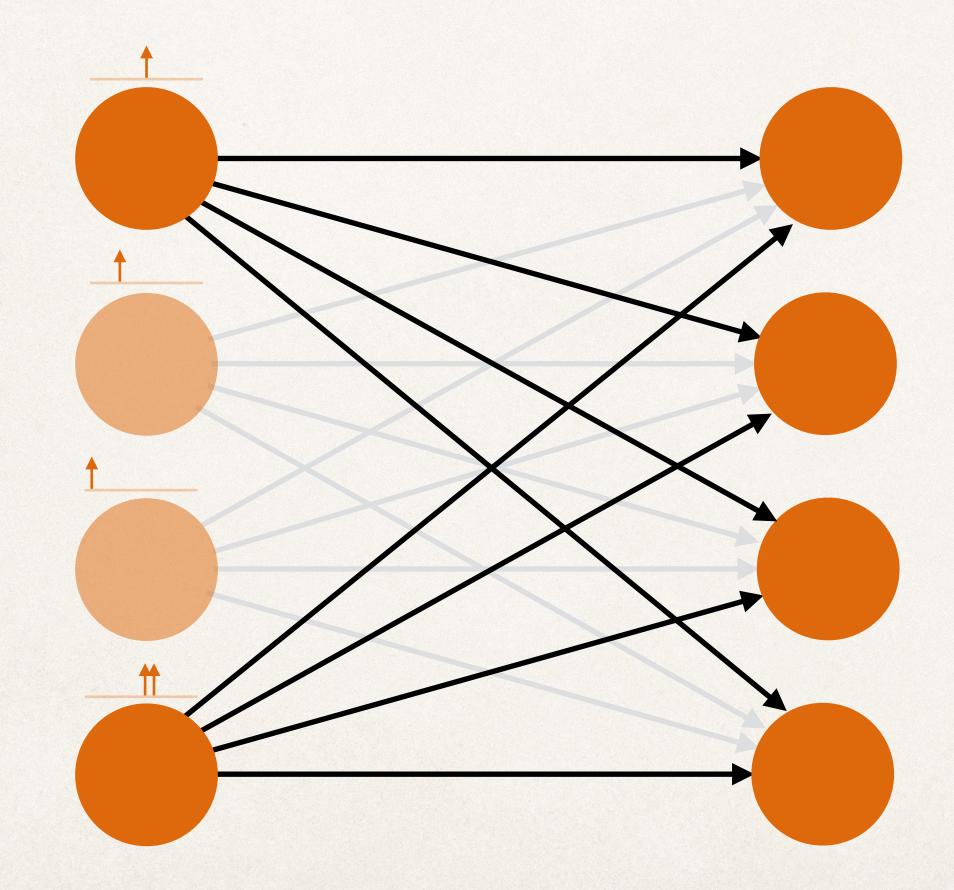
Minimizing energy: Temporal sparsity



 $E_{op} = N_{active} N_{conn}$ $= (\rho_{active} N)(\rho_{conn} N)$



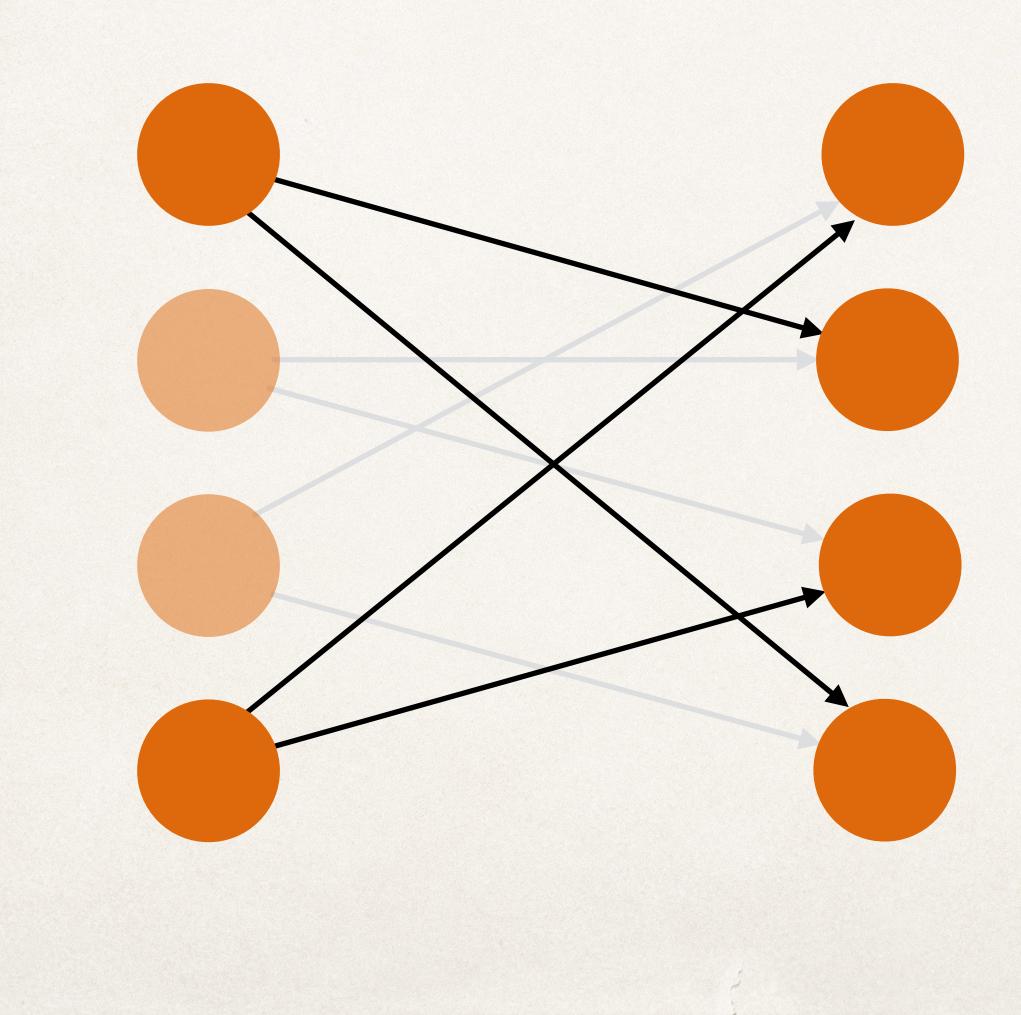
Temporal sparsity: Spikes



 $E_{op} = N_{active} N_{conn}$ $= (\rho_{active} N)(\rho_{conn} N)$



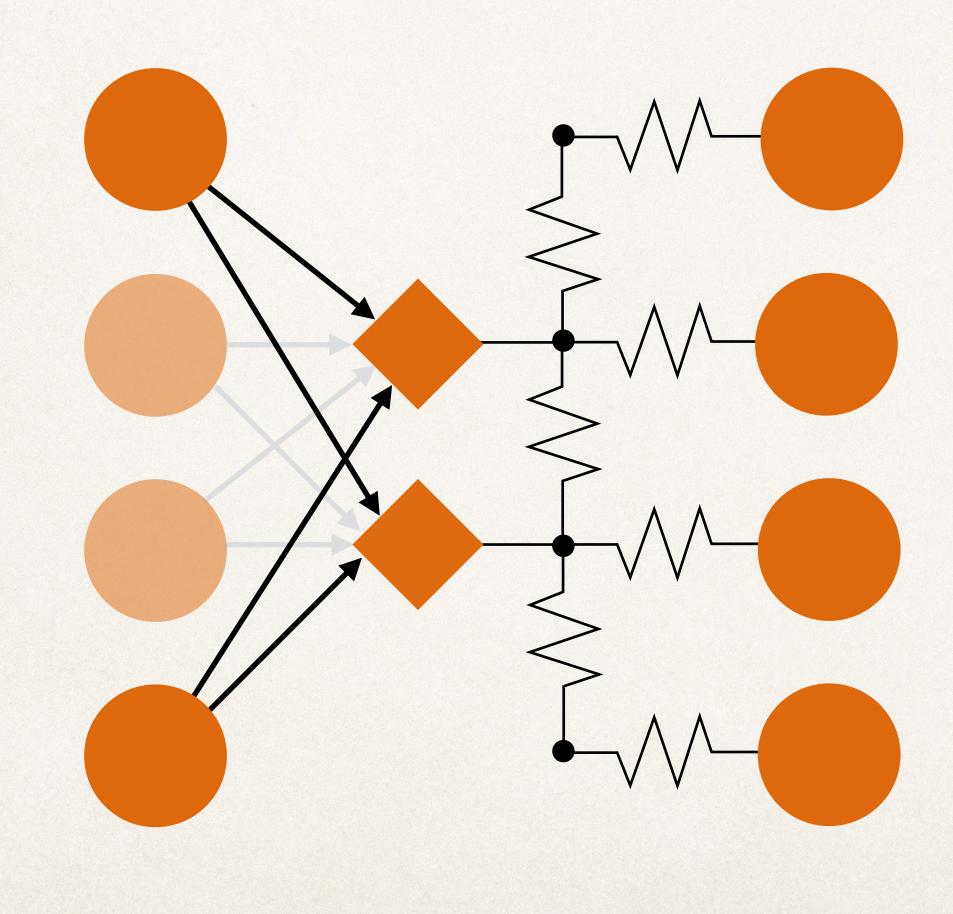
Minimizing energy: Spatial sparsity



 $E_{op} = N_{active} N_{conn}$ $= (\rho_{active} N) (\rho_{conn} N)$



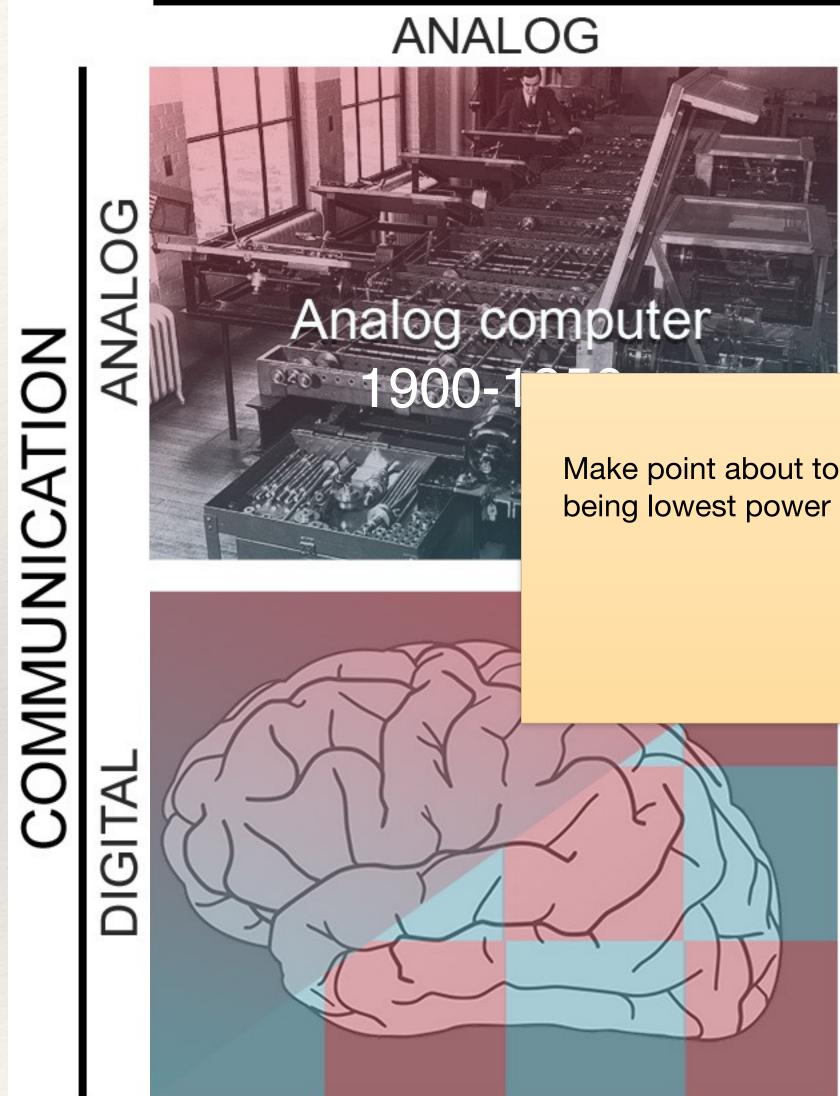
Spatial sparsity: Analog convolving



$E_{op} = N_{active} N_{conn}$ $= (\rho_{active} N) (\rho_{conn} N)$



COMPUTATION



DIGITAL



Make point about top-left corner





Digital versus Analog: 1 day versus 1000 yrs

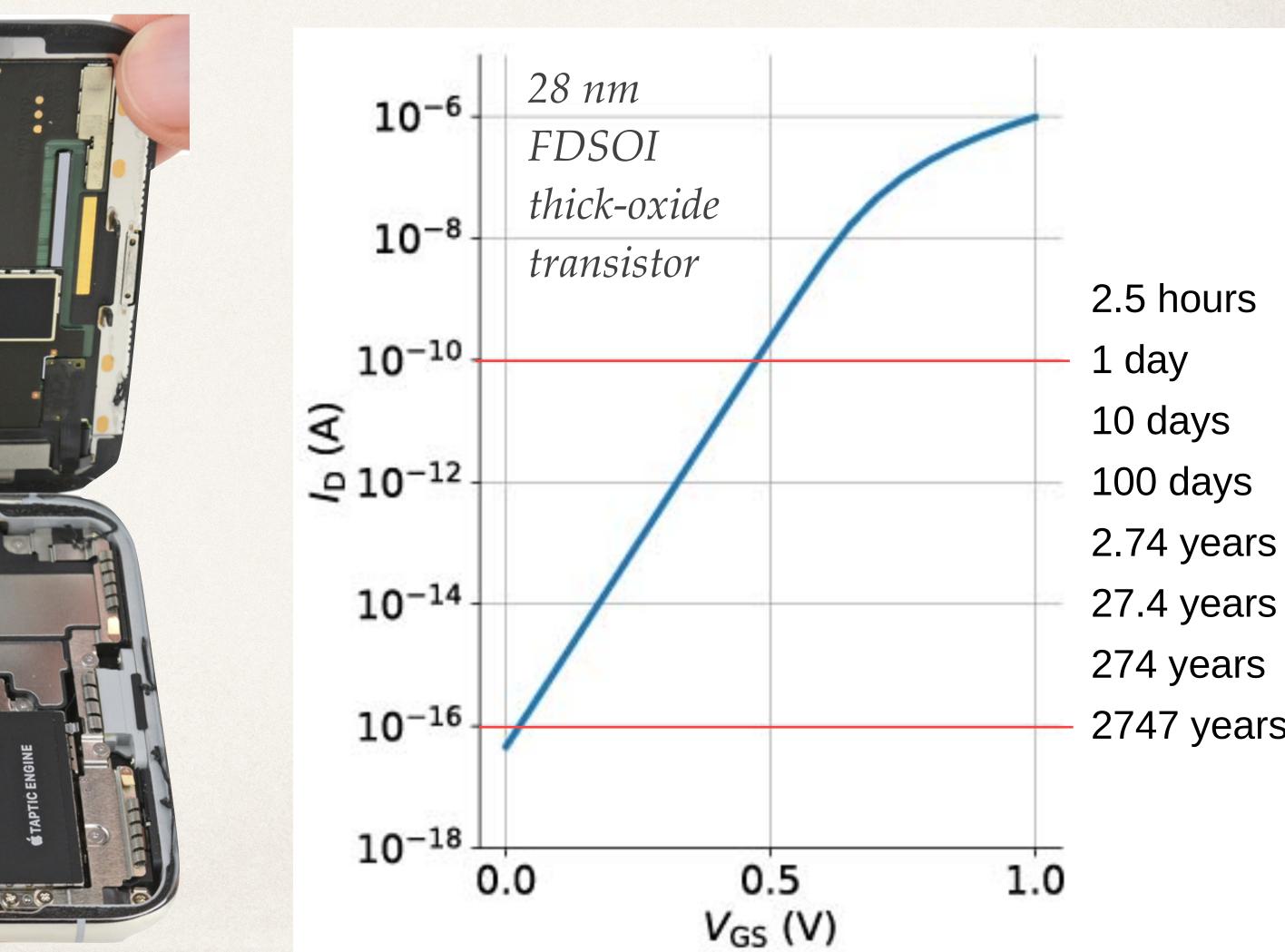
4.3B-transistor processor 10.35Wh battery

land -

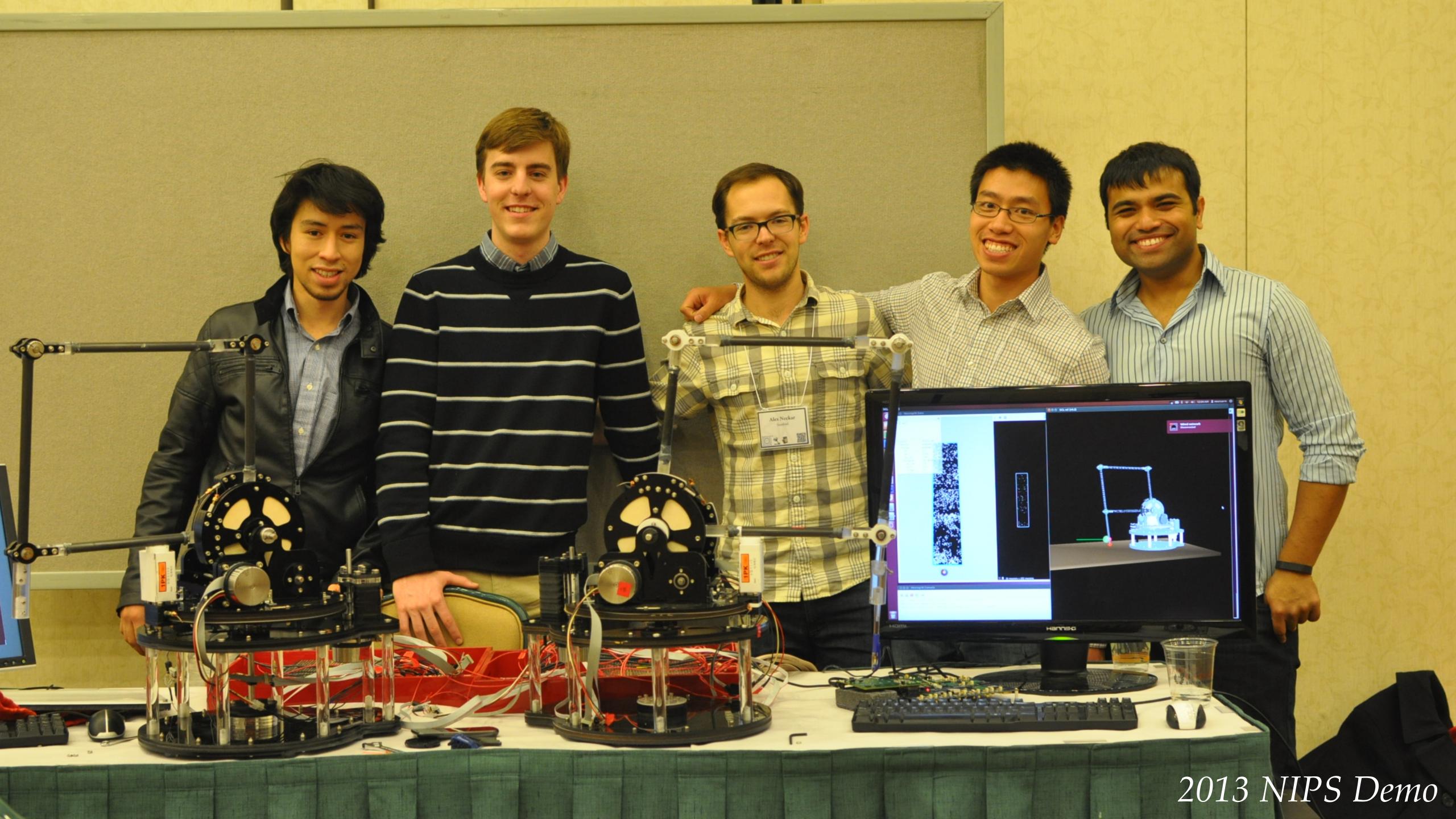
Pro anti alla

-i-ion 2716mAth Pple Japa

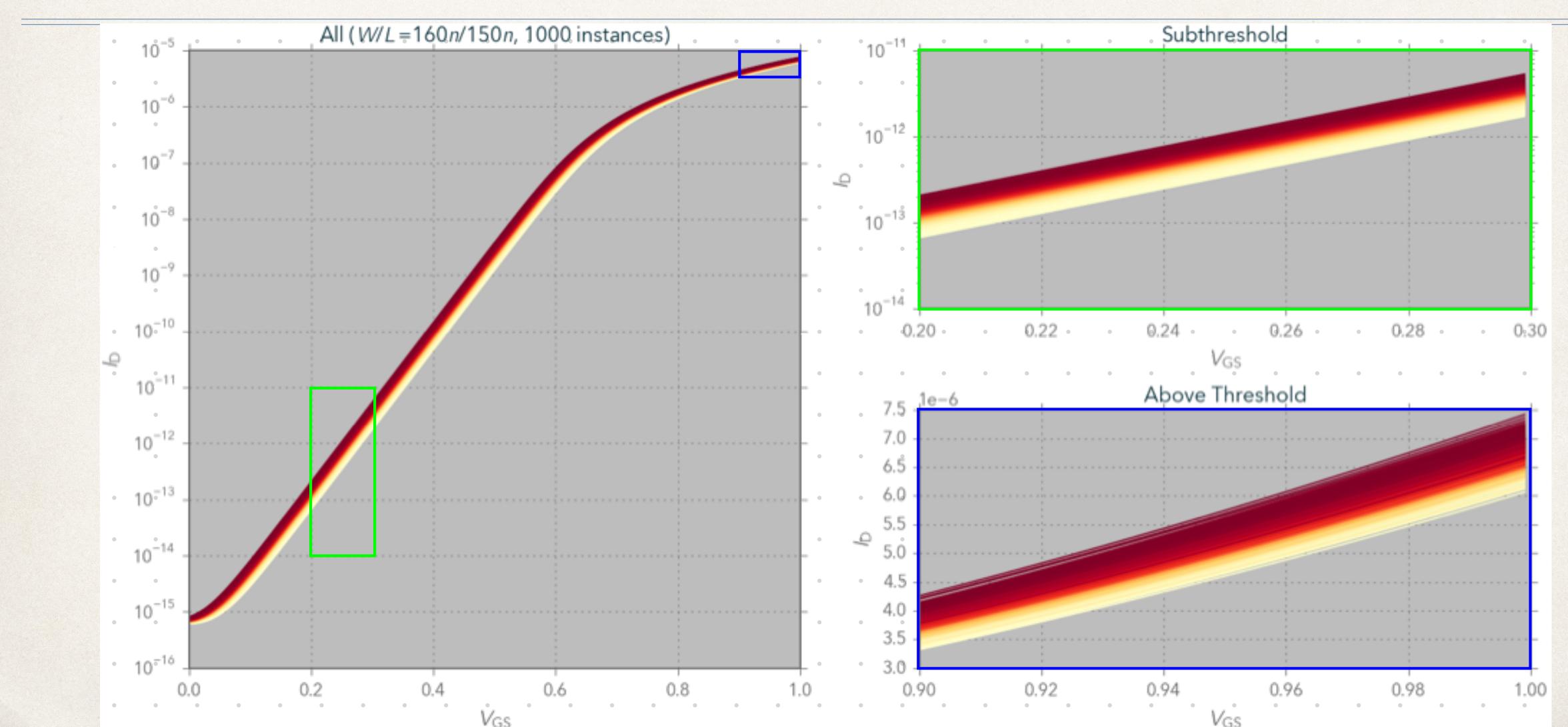
CYL US MH45584





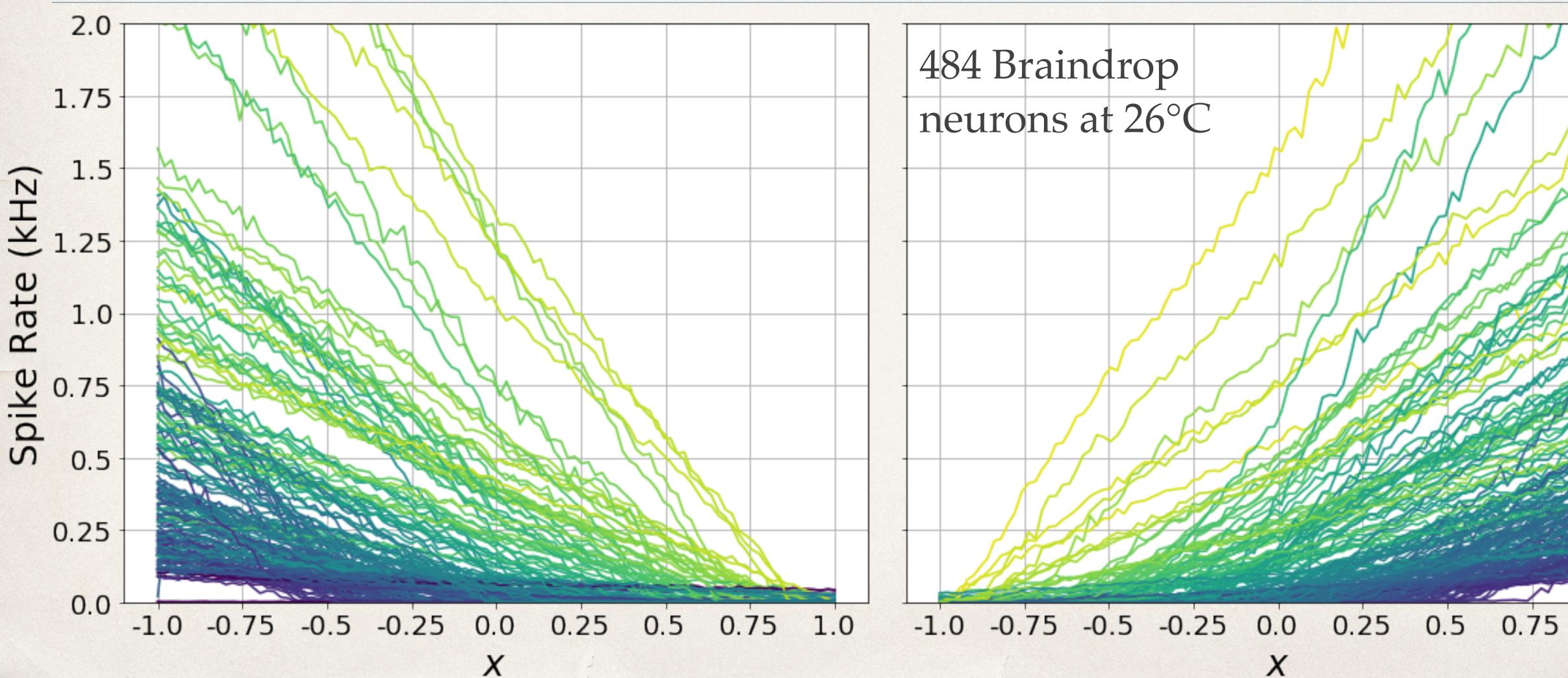


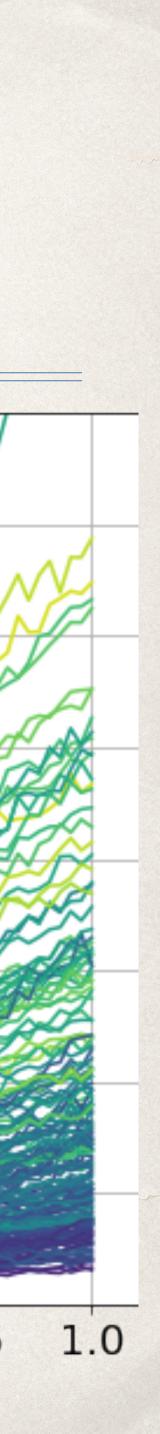
Analog Challenge I: Heterogeneity



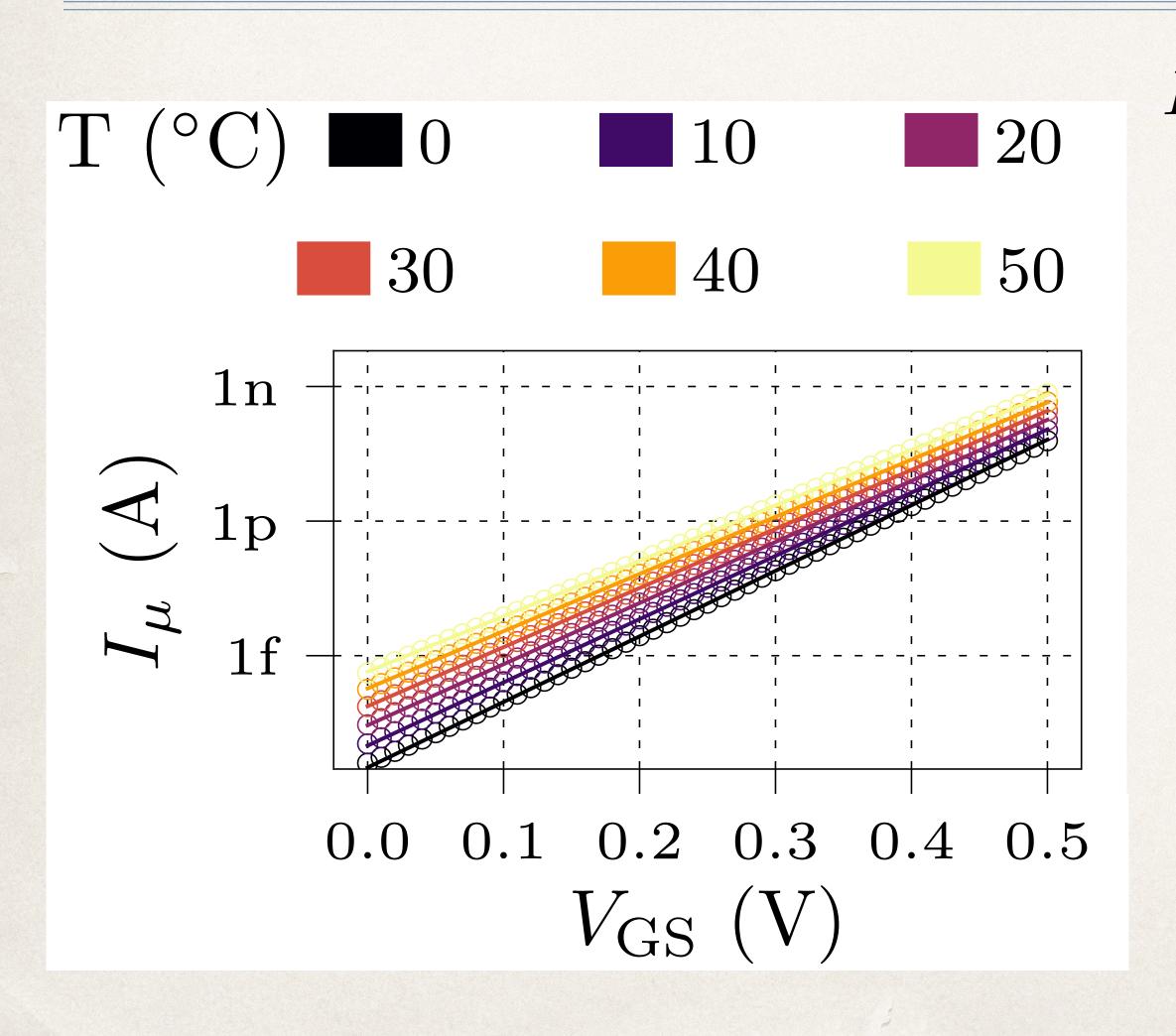


Silicon neurons' tuning-curves (Braindrop)





Analog Challenge I: Thermal Sensitivity



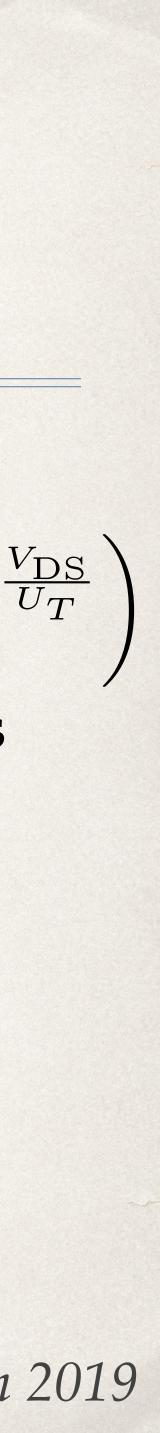
$$I_{\mu}(T) = I_{0_{\text{nom}}} e^{\langle \gamma_1 \rangle \left(1 - \frac{T_{\text{nom}}}{T}\right)} e^{\frac{(1 - \kappa) V_{\text{BS}}}{U_T}} \\ \times e^{\frac{\kappa V_{\text{GS}}}{U_T}} e^{\left(\lambda_1 \frac{T_{\text{nom}}}{T} + \lambda_2\right) \Delta V_{\text{DS}}} \left(1 - e^{-\frac{\kappa V_{\text{BS}}}{U_T}}\right)$$

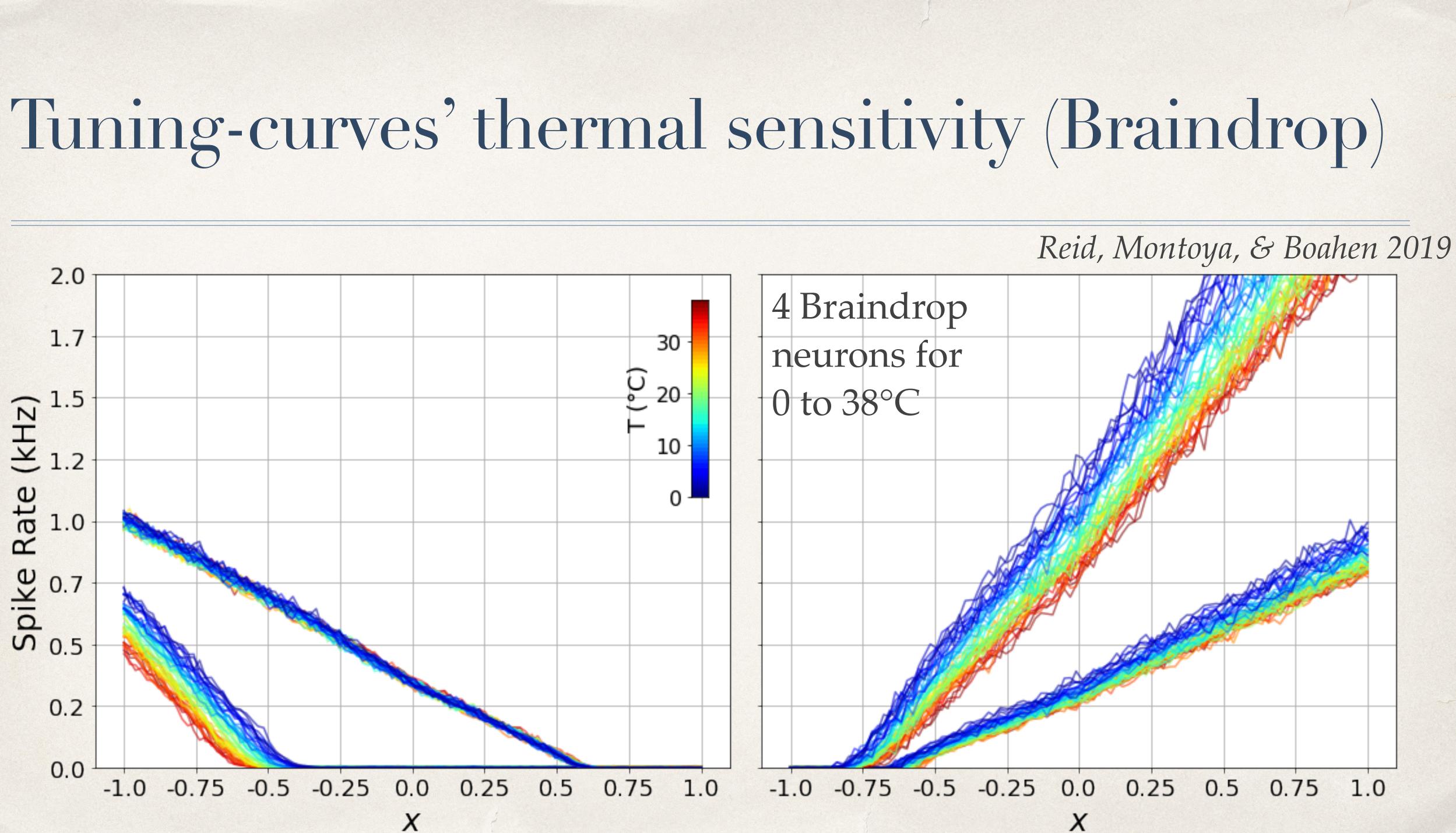
* A subthreshold transistor's current (I_{μ}) is exponentially sensitive to temperature

* *T* is the absolute temperature

• $U_T = kT/q$ is the thermal voltage

Across a 50°C range, the current changes
 by 1.5 to 3 decades
 Benjamin & Boahen 2019

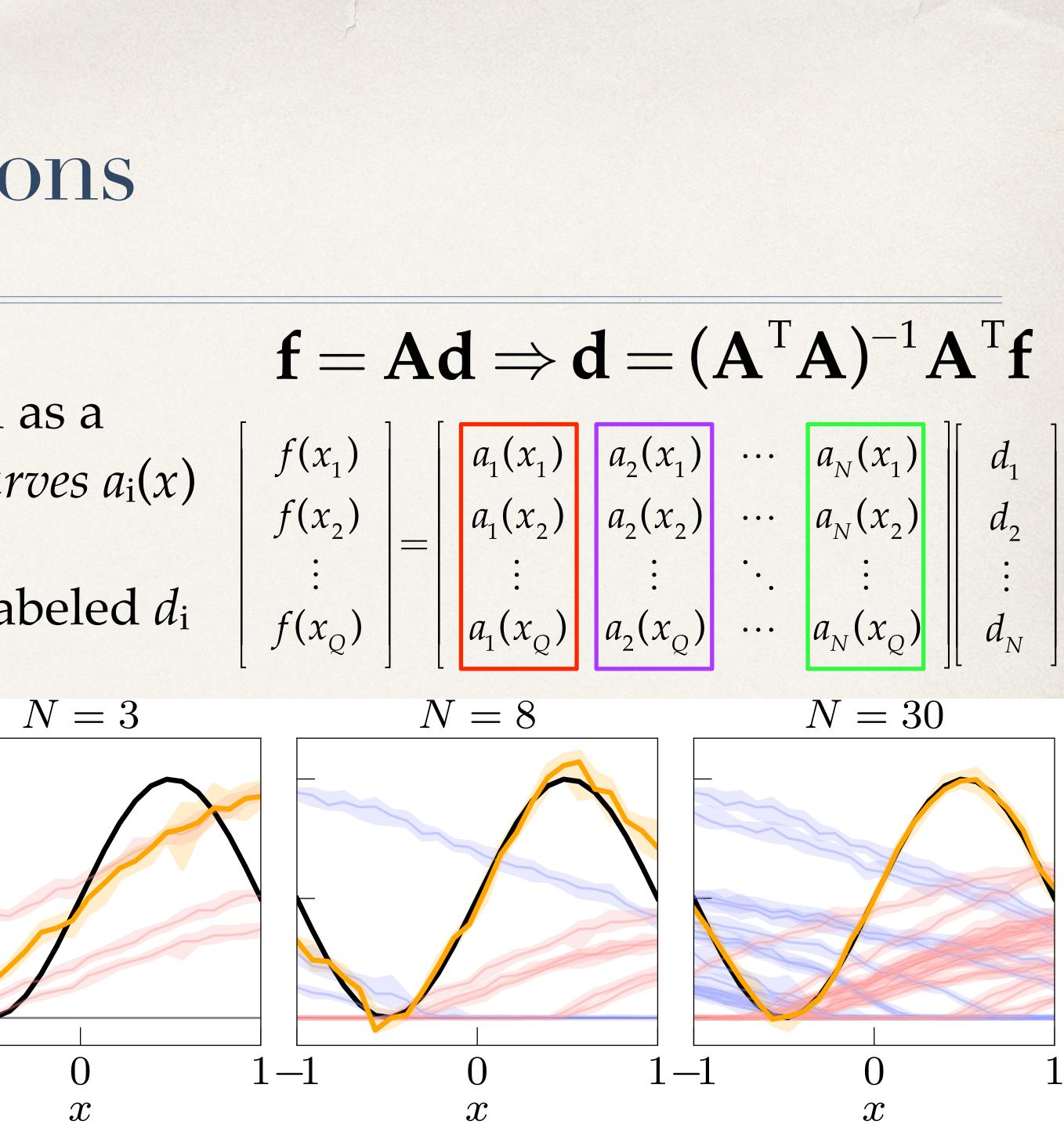




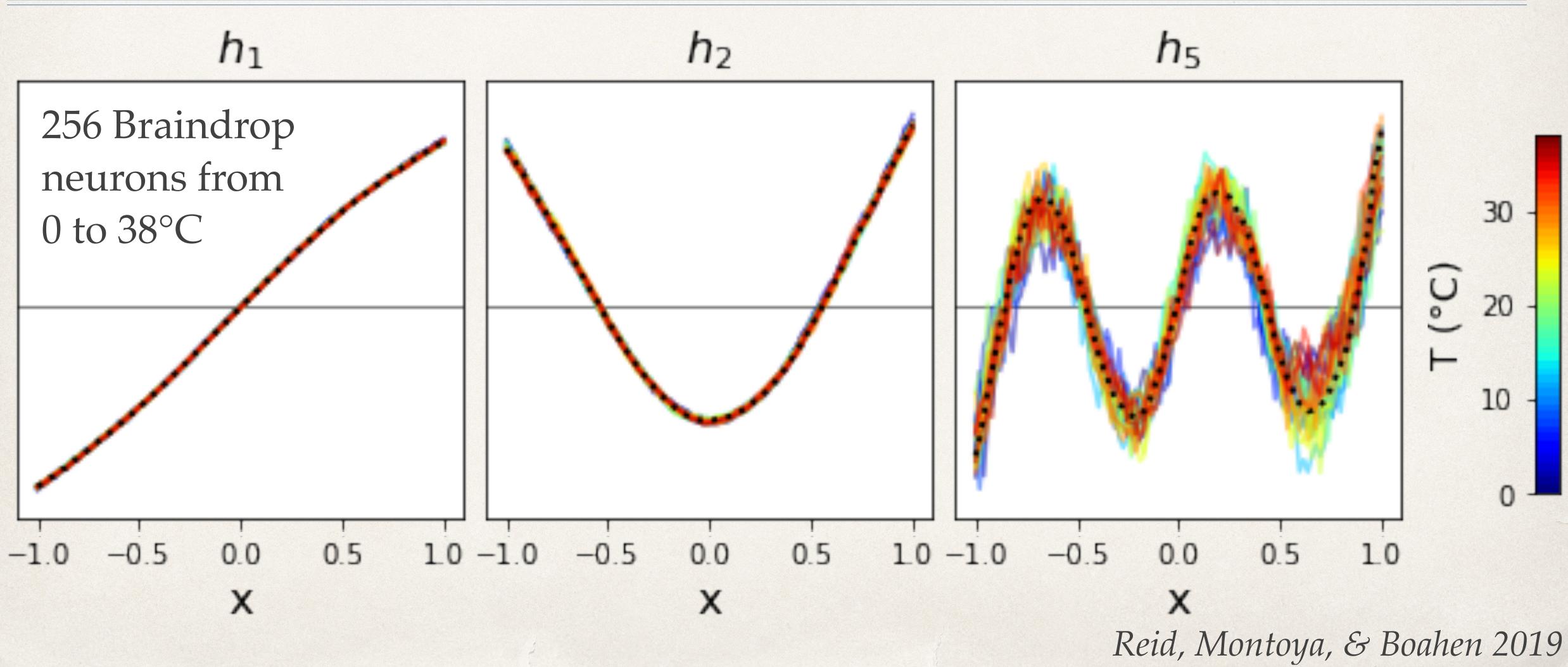
Approximating functions

- The desired function *f*(*x*) is expressed as a weighted sum of the neural *tuning curves a_i(x*)
- The weights—called decoders—are labeled d_i

$$\dot{V}$$
 1.0
 \dot{V} 0.5
 \dot{S} 0.5
 \dot{S} 0.0
-1

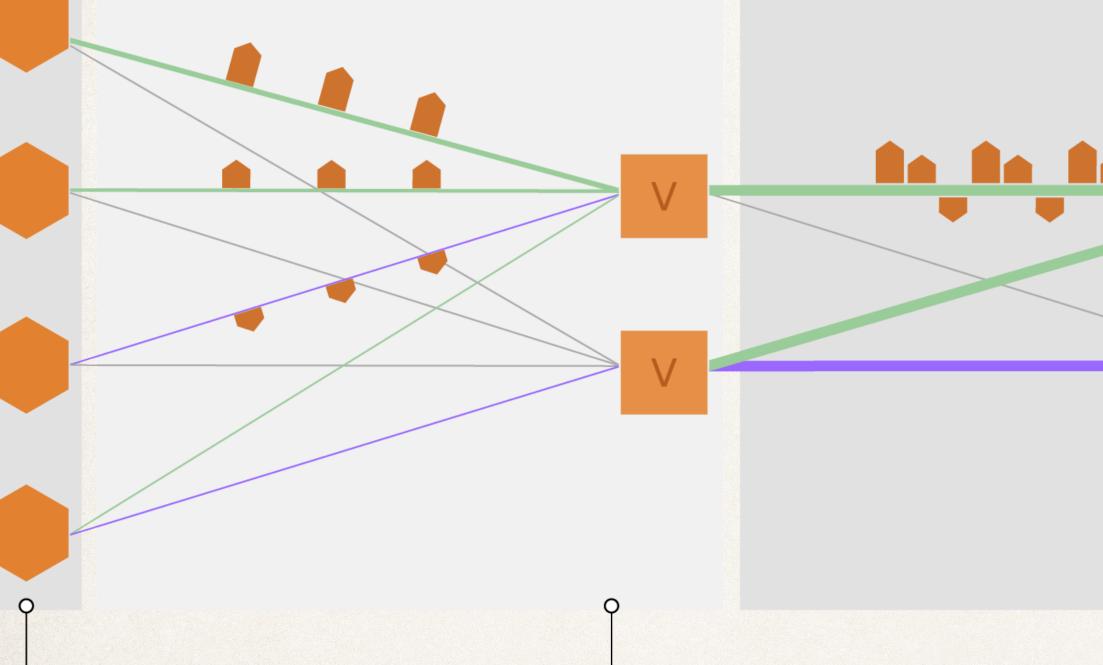


Thermally robust computation (Braindrop)





NEF: Decode-Transform-Encode





$\langle \delta_{x_i} \rangle_t = [0, \alpha_i (I_i + \beta_i)]$

Somas emit unit-area deltas δ_{x_i} at rates $\langle \delta_{x_i} \rangle_t$ dictated by their input current I_i .

2 Decode

 $\delta_{y_j} = \sum_i D_{ji} \delta_{x_i}, D \in \mathbb{R}^{D \times N}$

Deltas are then scaled by their decode weight and merged together.

Eliasmith & Anderson 2003

3 Transform

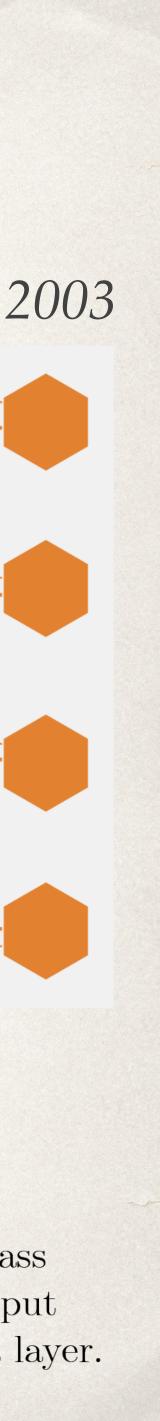
 $\delta_{z_k} = \sum_j T_{kj} \delta_y, T \in \mathbb{R}^{D \times D}$

Transform works the same way as Decode.

4 Encode

$$\tau \dot{I}_l = -I_l + \sum_k E_{lk} \delta_{z_k}, E \in \mathbb{R}^{N \times D}$$

Synaptic filters superpose and low-pass filter weighted deltas to produce output currents (I_l) that feed the next soma layer.



Digital thinning and analog convolving

1 Spike

 $\langle \delta_{x_i} \rangle_t =$ $[0, \alpha_i(I_i + \beta_i)]$

Somas emit delta trains (as in Figure 2). 2 Decode

$$\left\langle \delta_{y_j} \right\rangle_t = \sum_i D_{ji} \left\langle \delta_{x_i} \right\rangle_t \\ D \in [-1, 1]^{D \times N}$$

Weighted deltas are accumulated to produce a stream of unit-area deltas. 3

in this example).

Transform

 $\langle \delta_{z_k} \rangle_t = \sum_j T_{kj} \left\langle \delta_{y_j} \right\rangle_t$ $T \in [-1,1]^{D \times D}$

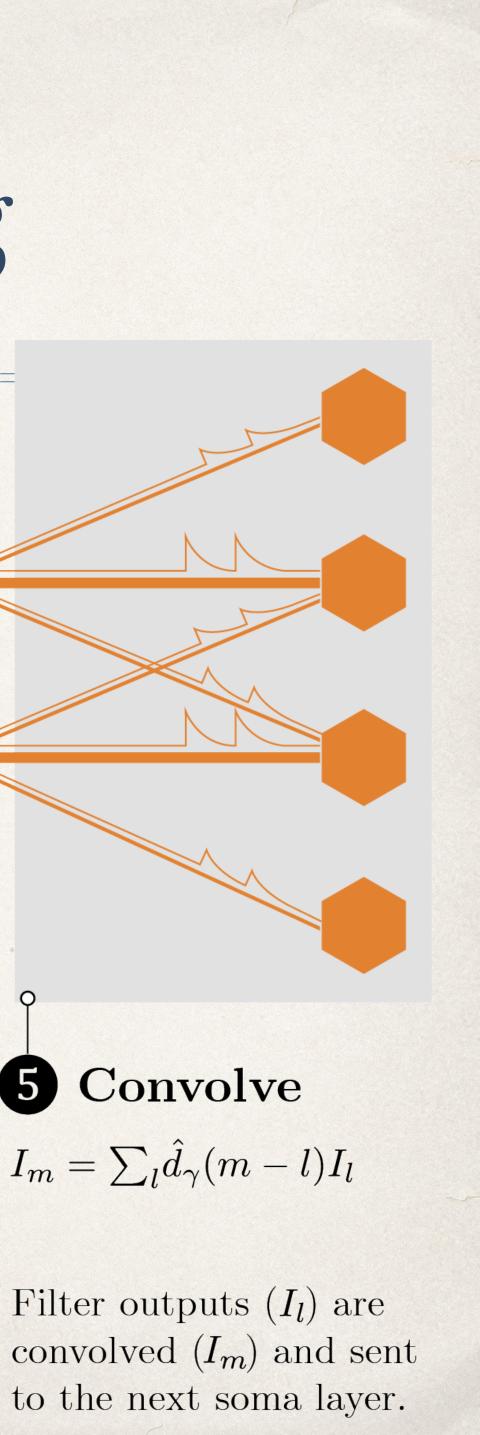
Transform still works the same as Decode $(T_{kj}=1)$

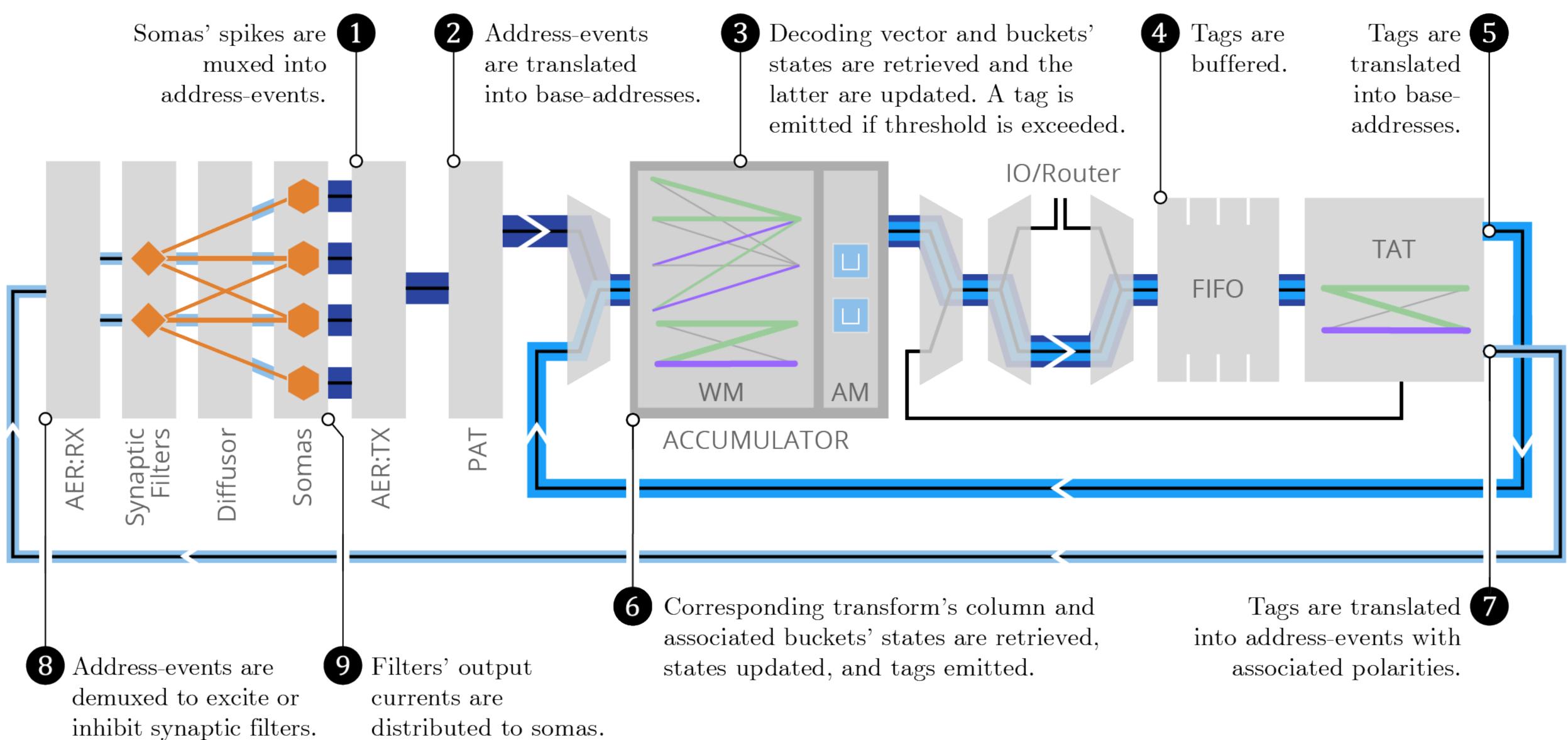
4 Sparse Encode

$$\tau I_l = -I_l + \sum_k S_{lk} \delta_{z_k}$$
$$S \in \{-1, 0, 1\}^{N \times D}$$

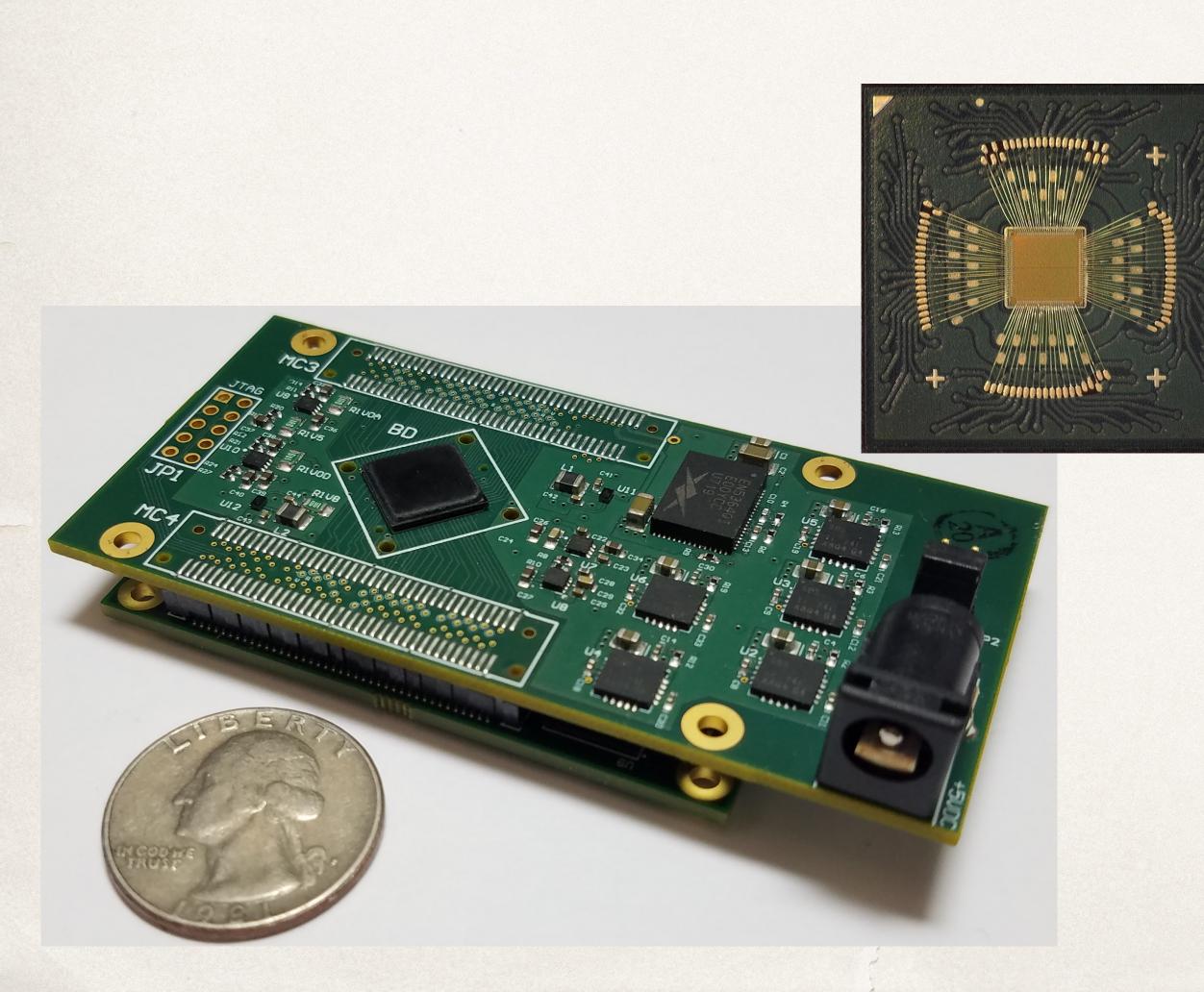
Each accumulator's deltas are sent to a subset of synaptic filters (tap-points). Filter outputs (I_l) are convolved (I_m) and sent to the next soma layer.

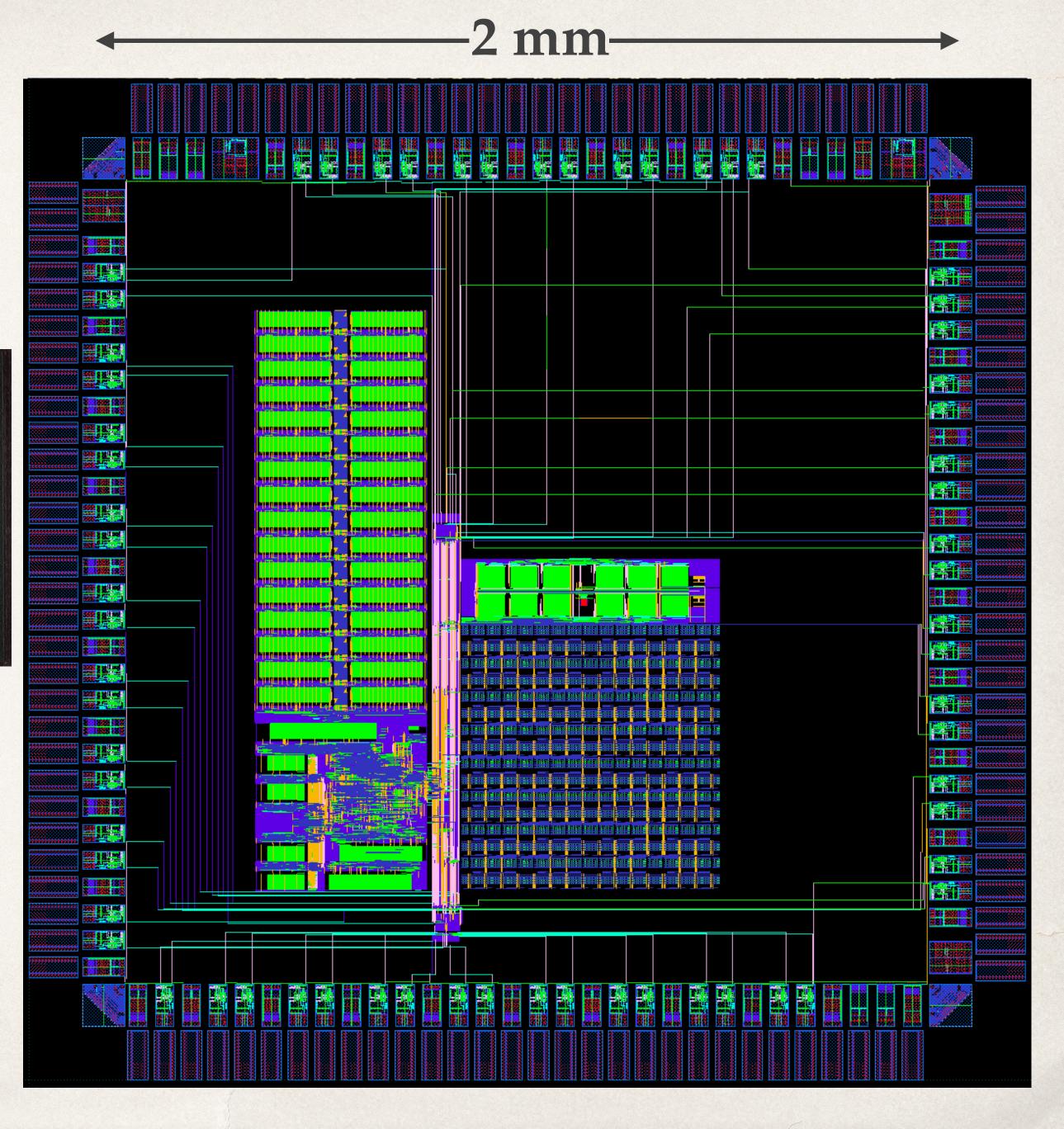
5 Convolve





Braindrop: 4096 neurons in 28nm FDSOI CMOS



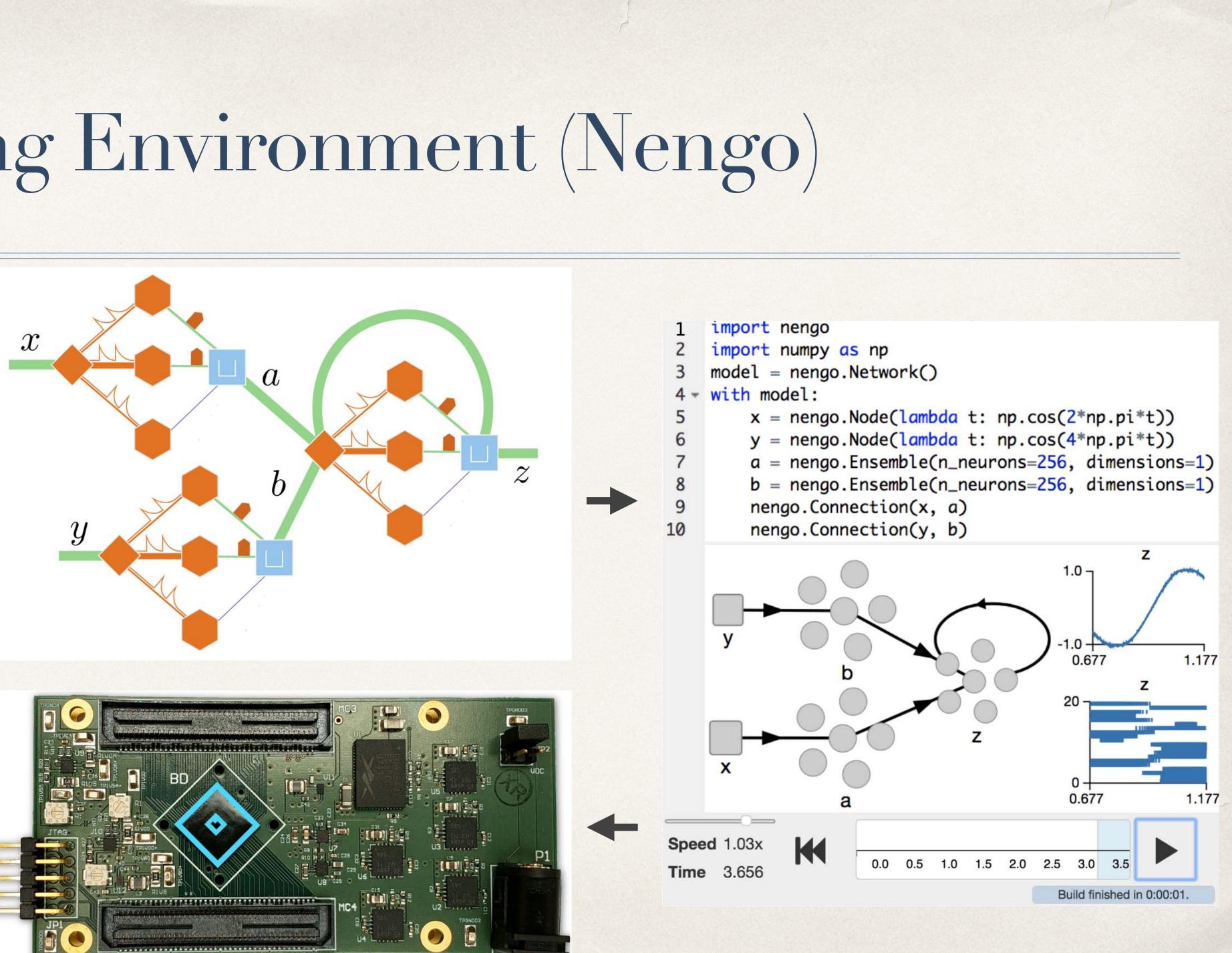


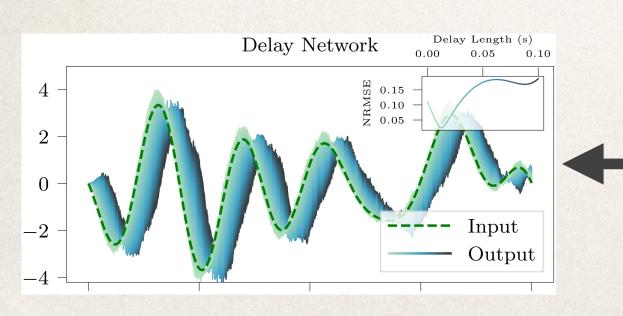
Programming Environment (Nengo)

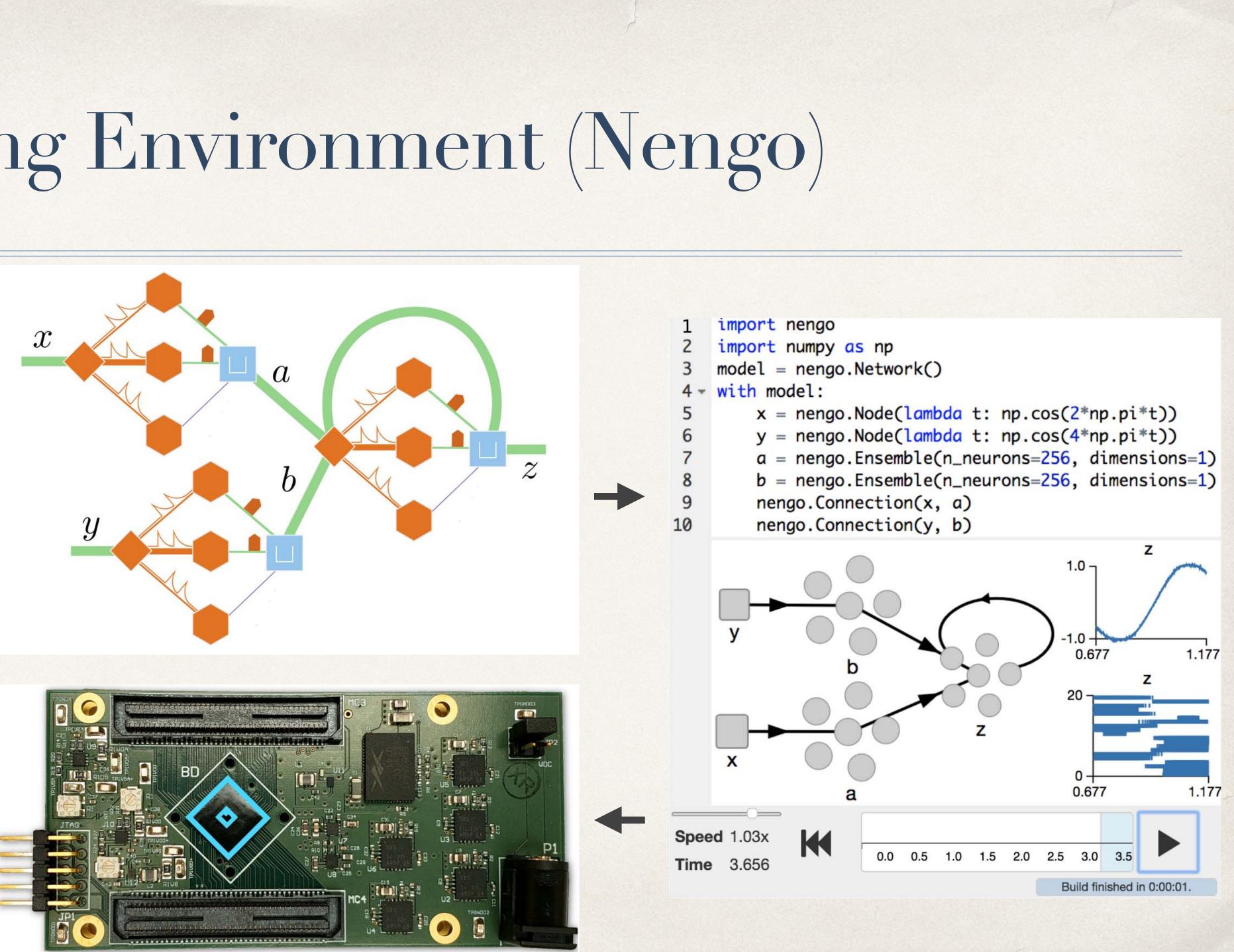
$$a = f(x)$$

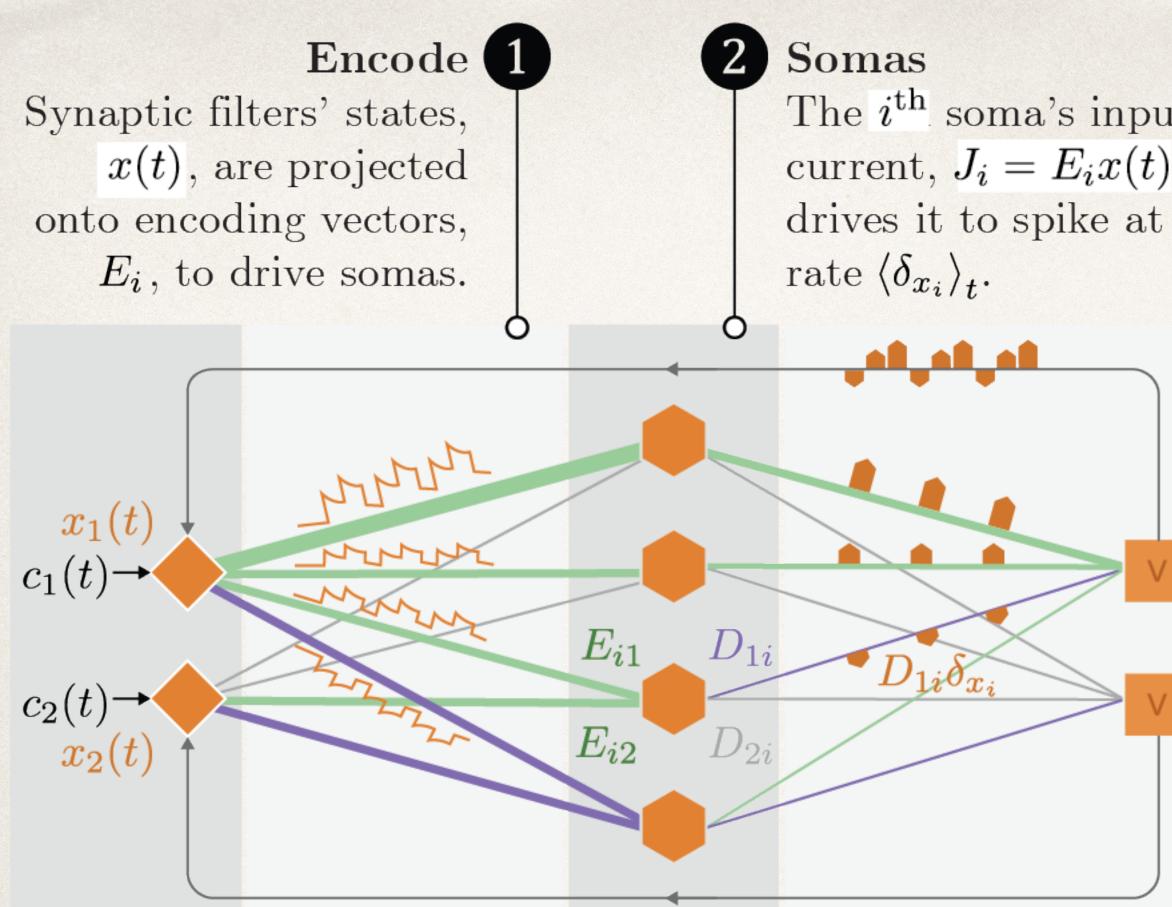
$$b = g(y)$$

$$\dot{z} = h(z) + a + b$$









Decode

Deltas with area equal to components of the neuron's decoding vector, D_i^{T} , replace spikes.

4 Synaptic Filters

 \mathbf{O}

Merged delta trains are lowpass filtered. As a result, $\tau_{syn}\dot{x}(t) + x(t) = \sum_i D_i^T \delta_{x_i} + c(t)$, where c(t) is a vector of injected currents.

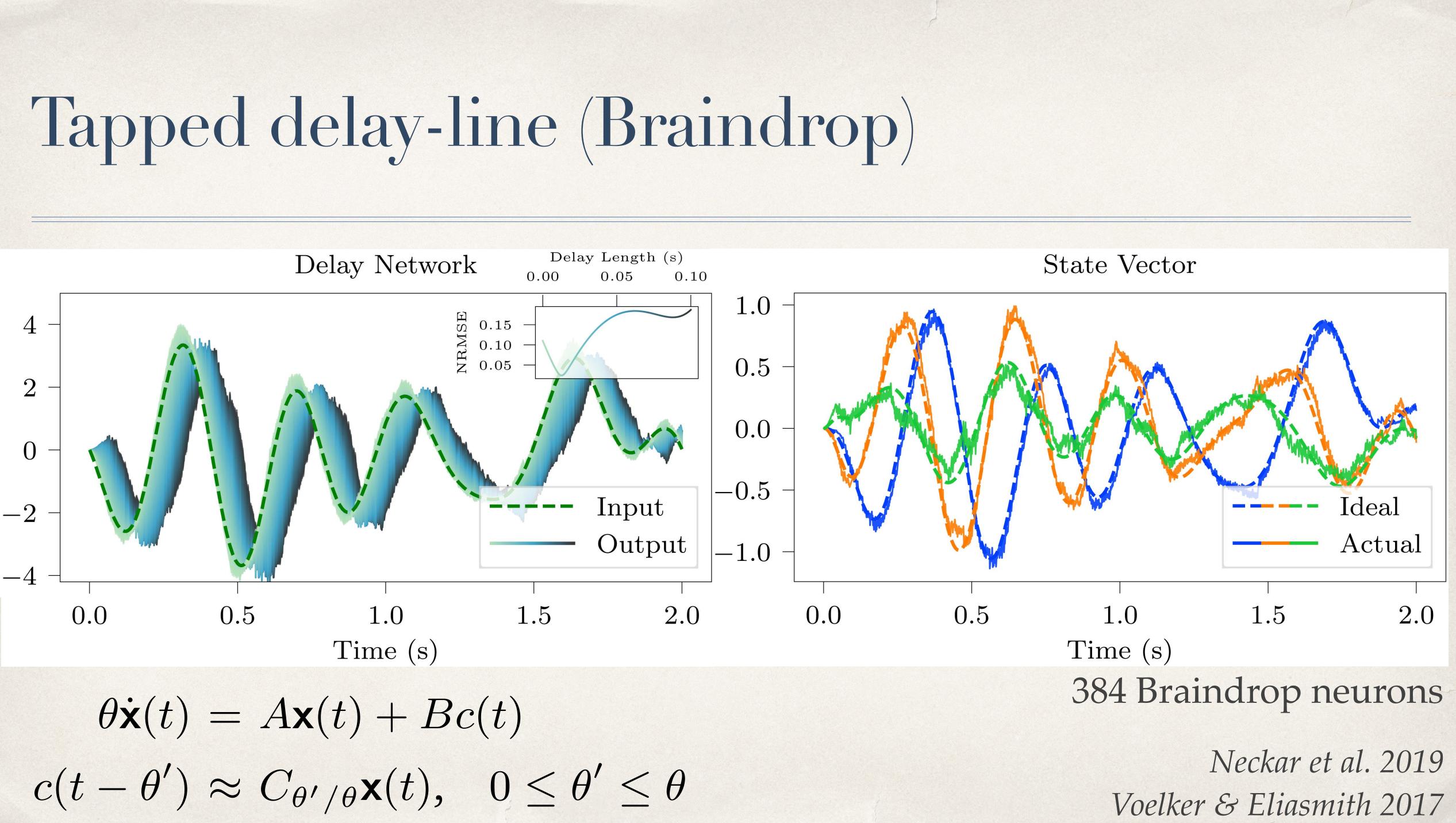
* To emulate the dynamical system

$$au_{dyn}\dot{x}(t) = f(x) + u(t)$$

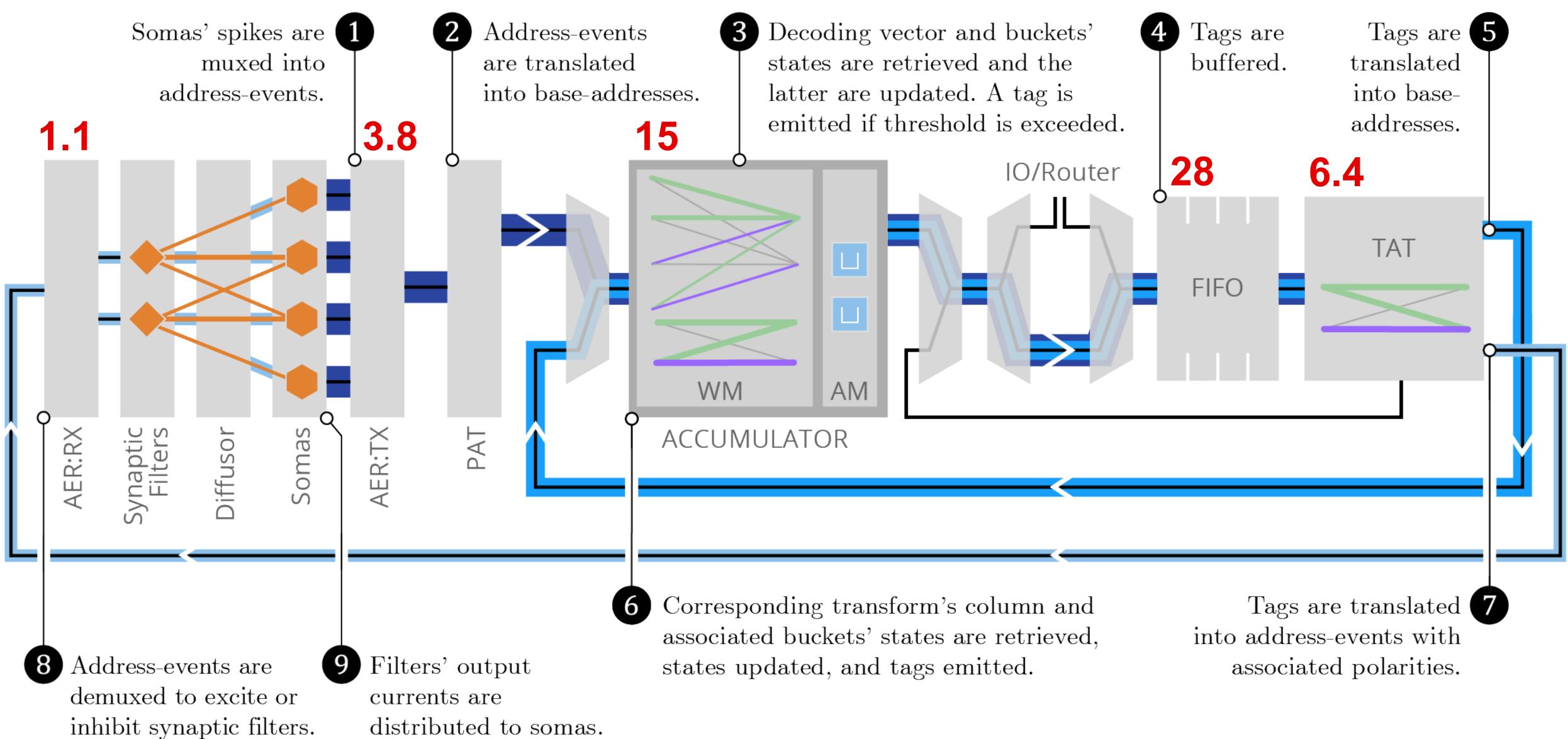
* Choose decoding weights such
that, after synaptic filtering,
 $\sum_i D_i^T \delta_{x_i} \approx \tau_{syn}/\tau_{dyn} f(x) + x$
* And set
 $c(t) = \tau_{syn}/\tau_{dyn} u(t)$

Eliasmith & Anderson 2003



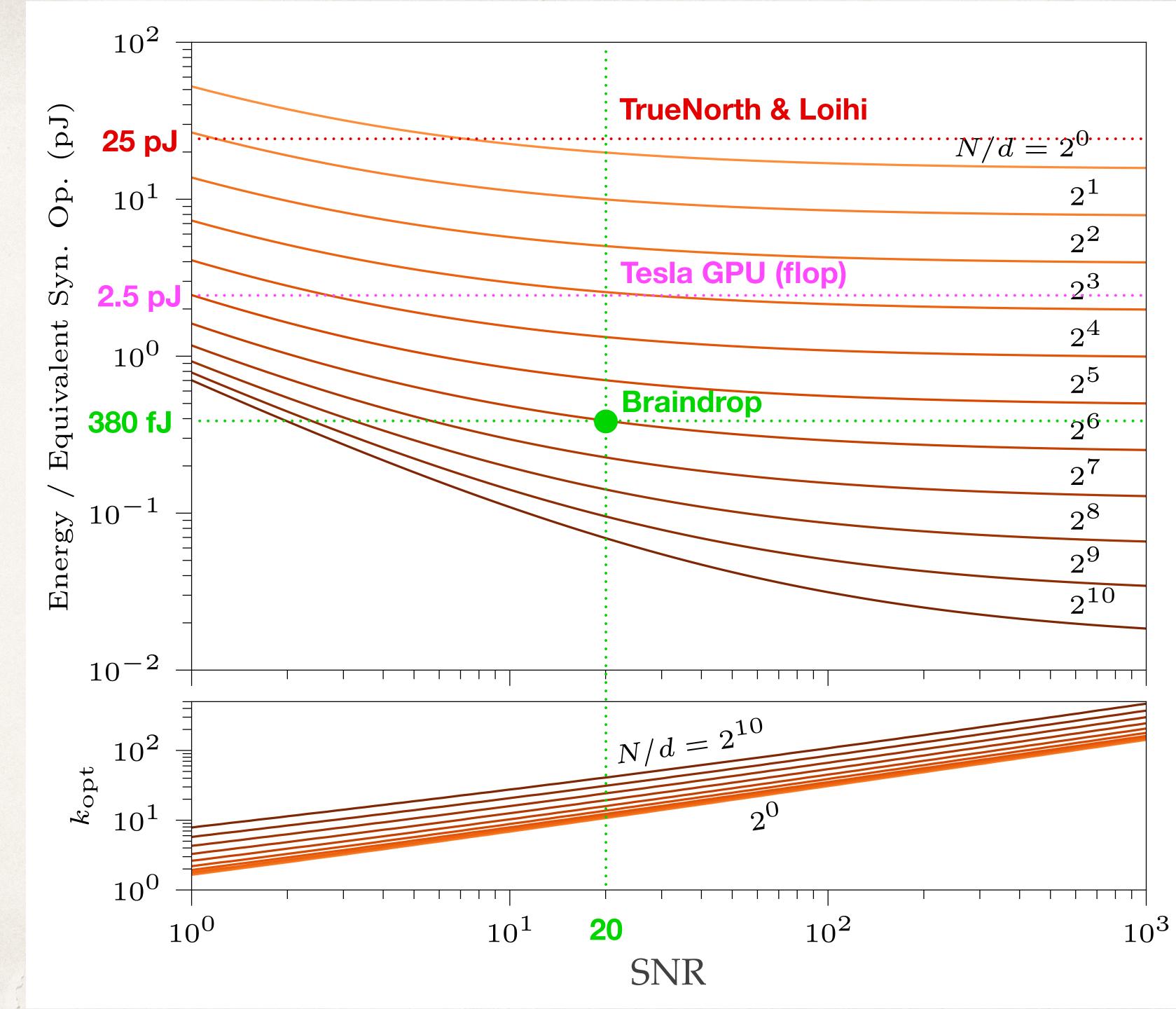


Measured Energy/op (pJ)



 Analog convolving fans out *d* spike-trains to *N* neurons; <u>sparsifies</u> <u>spatially by *d*/*N*</u>

Digital thinning lets
 one per SNR spikes
 through; sparsifies
 temporally by 1/SNR



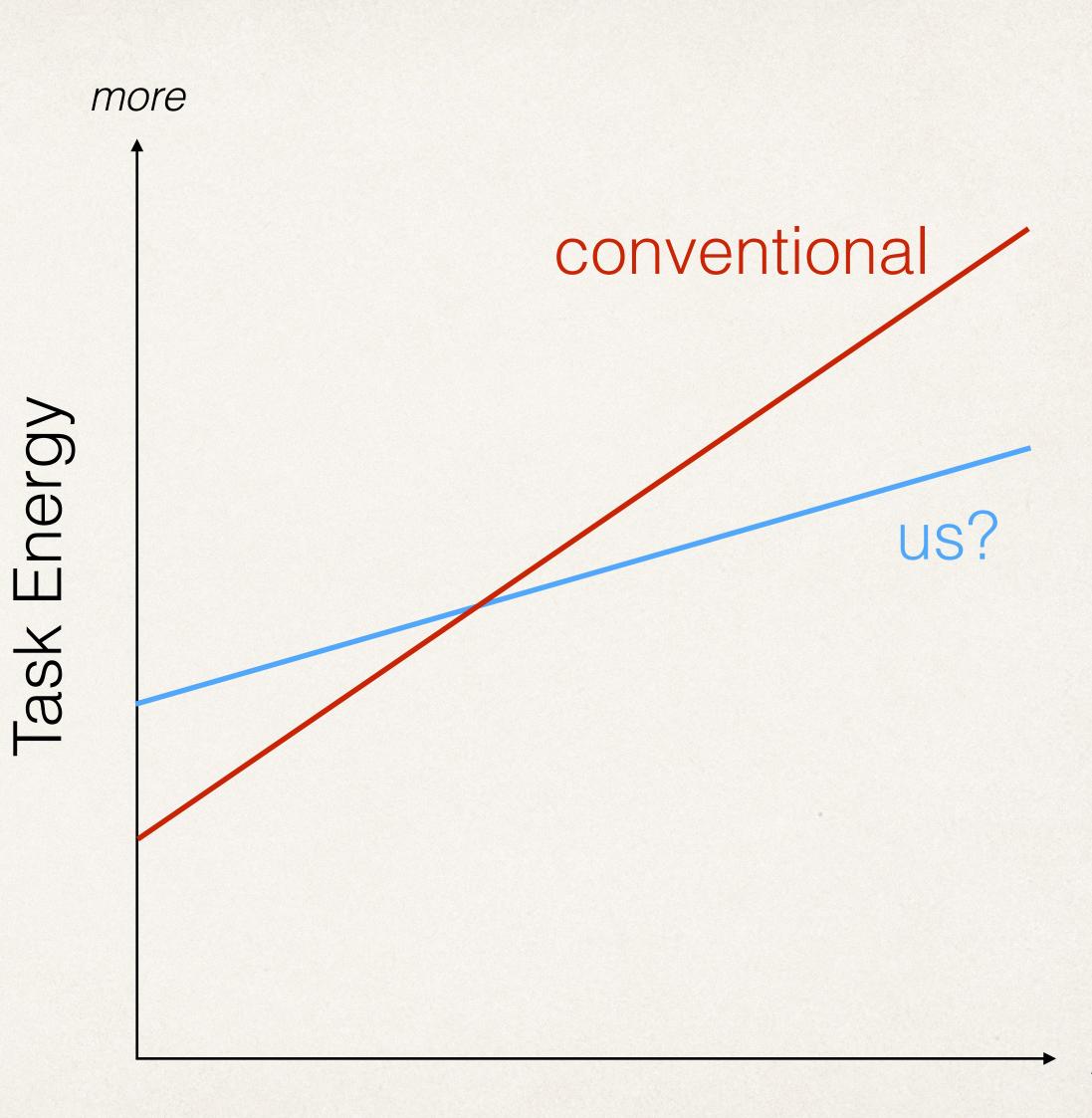
Task performance

Two components:

- Network design
- Hardware design

 $E_{sys}(task) = E_{HW}(R_{net}(task))$

 $E_{op} = N_{active} N_{conn}$ $(\rho_{active}N)(\rho_{conn}N)$ _____



Task Complexity/Performance





Acknowledgments













Students & Staff Max Kanwal Scott Reid E. Kauderer-Abrams Jonathan Timcheck **Recent Alumni** Ben Benjamin Alex Neckar Sam Fok Nick Oza Ashok Cutkosky John Aguayo Tatiana Engel Samir Menon Peiran Gao Nick Steinmetz Rodrigo Alvarez

Collaborators Stanford Krishna Shenoy Tirin Moore Oussama Khatib Waterloo Chris Eliasmith Terry Stewart Aaron Voelker **Cornell & Yale** Rajit Manohar Ned Bingham Silvia Ferarri Taylor Clawson Funding NIH Pioneer, TR01 **ONR: C. Baatar**

To learn more ...

🔚 J Dethier, P Nuyujukian, C Eliasmith, T Stewart, S A Elassaad, K V Shenoy, 🛛 💻 and K Boahen, A Brain-Machine Interface Operating with a Real-Time Spiking Neural Network Control Algorithm, Advances in Neural Information Processing Systems 24, Curran Associates, Inc., pp 2213-21, 2011.

S Choudhary, S Sloan, S Fok, A Necker, E Trautmann, P Gao, T Stewart, C Eliasmith, and K Boahen, Silicon Neurons that Compute, International Conference on Artificial Neural Networks, LNCS vol VV, pp 121-128, Springer, Heidelberg, 2012.

S Menon, S Fok, A Neckar, O Khatib, and K Boahen, Controlling Articulated Robots in Task-Space with Spiking Silicon Neurons, IEEE International Conference on Biomedical Robotics and Biomechatronics (BioRob), IEEE Press, pp 181-186, 2014.

K Boahen, **A Neuromorph's Prospectus**, Computing in Science & Engineering, vol 19, no 2, pp 14-28, IEEE Computer Society, Los Alamitos CA, USA, 2017.

E Kauderer-Abrams, A Gilbert, A Voelker, B Benjamin, and T C Stewart, and K Boahen, A Population-Level Approach to Temperature Robustness in Neuromorphic Systems, IEEE International Symposium on Circuits and Systems (ISCAS), Baltimore MD, 2017.

A R Voelker, B V Benjamin, T C Stewart, K Boahen, and C Eliasmith, **Extending the Neural Engineering Framework for Nonideal Silicon Synapses**, *IEEE International Symposium on Circuits and Systems* (ISCAS), Baltimore MD, 2017.

E Kauderer-Abrams and K Boahen, Calibrating Silicon-Synapse **Dynamics using Time-Encoding and Decoding Machines**, *IEEE* International Symposium on Circuits and Systems (ISCAS), Baltimore MD, 2017.

Proceedings of the IEEE, Jan 2019



Braindrop: A Mixed-Signal Neuromorphic Architecture With a Dynamical Systems-Based **Programming Model**

This paper provides an overview of a current approach for the construction of a programmable computing machine inspired by the human brain.

By Alexander Neckar^(D), Sam Fok^(D), Ben V. Benjamin, Terrence C. Stewart, Nick N. Oza, AARON R. VOELKER^(D), CHRIS ELIASMITH^(D), RAJIT MANOHAR^(D), Senior Member IEEE, AND KWABENA BOAHEN, Fellow IEEE





